

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY	TYPICAL POWER DISSIPATION
'95A	36 MHz	195 mW
LS95B	36 MHz	65 mW

SN5495A, SN54LS95B . . . J OR W PACKAGE
 SN7495A . . . N PACKAGE
 SN74LS95B . . . D OR N PACKAGE
 (TOP VIEW)

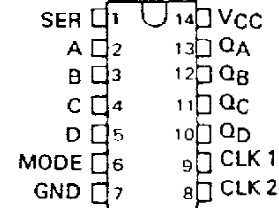
description

These 4-bit registers feature parallel and serial inputs, parallel outputs, mode control, and two clock inputs. The registers have three modes of operation:

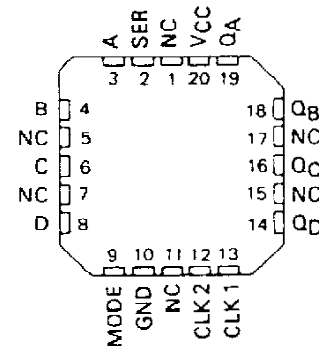
- Parallel (broadside) load
- Shift right (the direction Q_A toward Q_D)
- Shift left (the direction Q_D toward Q_A)

Parallel loading is accomplished by applying the four bits of data and taking the mode control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the clock-2 input. During loading, the entry of serial data is inhibited.

Shift right is accomplished on the high-to-low transition of clock 1 when the mode control is low; shift left is accomplished on the high-to-low transition of clock 2 when the mode control is high by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input C, etc.) and serial data is entered at input D. The clock input may be applied commonly to clock 1 and clock 2 if both modes can be clocked from the same source. Changes at the mode control input should normally be made while both clock inputs are low; however, conditions described in the last three lines of the function table will also ensure that register contents are protected.



SN54LS95B . . . FK PACKAGE
 (TOP VIEW)



NC - No internal connection

FUNCTION TABLE

MODE CONTROL	CLOCKS		INPUTS				OUTPUTS				
	2 (L)	1 (R)	SERIAL	PARALLEL				Q_A	Q_B	Q_C	Q_D
				A	B	C	D				
H	H	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	↓	X	X	a	b	c	d	a	b	c	d
H	↓	X	X	Q_B^{\dagger}	Q_C^{\dagger}	Q_D^{\dagger}	d	Q_{Bn}	Q_{Cn}	Q_{Dn}	d
L	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
L	X	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
L	X	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
↑	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↓	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	L	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
↑	H	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

[†]Shifting left requires external connection of Q_B to A, Q_C to B, and Q_D to C. Serial data is entered at input D.

H = high level (steady state), L = low level (steady state), X = irrelevant (any input, including transitions)

↓ = transition from high to low level, ↑ = transition from low to high level

a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.

Q_{A0} , Q_{B0} , Q_{C0} , Q_{D0} = the level of Q_A , Q_B , Q_C , or Q_D , respectively, before the indicated steady-state input conditions were established.

Q_{An} , Q_{Bn} , Q_{Cn} , Q_{Dn} = the level of Q_A , Q_B , Q_C , or Q_D , respectively, before the most-recent ↓ transition of the clock.

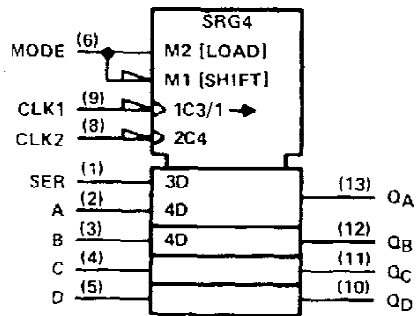
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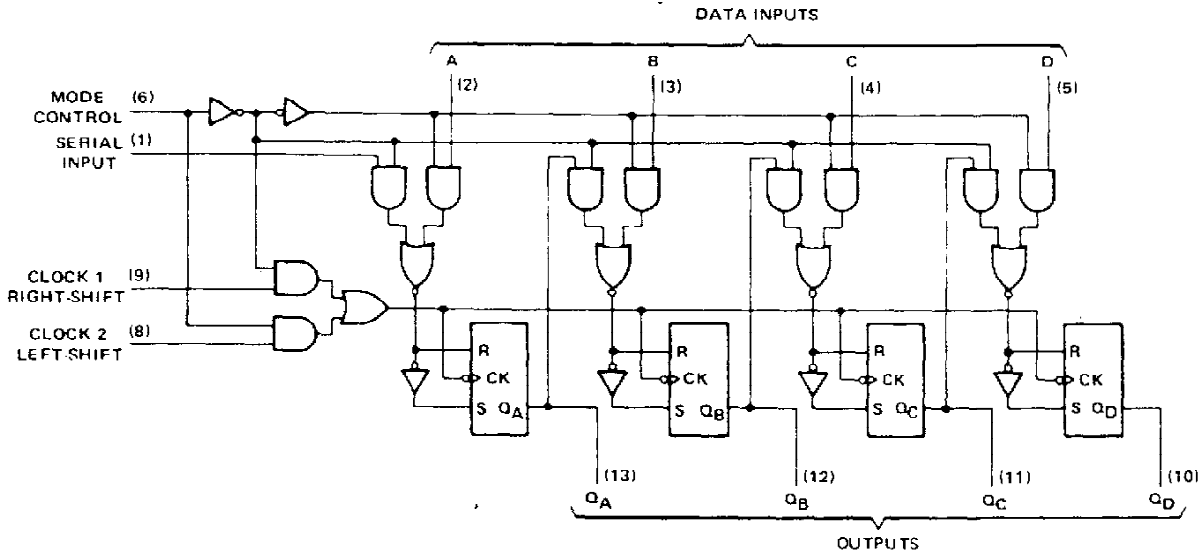
SN5495A, SN54LS95B, SN7495A, SN74LS95B
4-BIT PARALLEL-ACCESS SHIFT REGISTERS

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for D, J, N, and W packages.

logic diagram (positive logic)

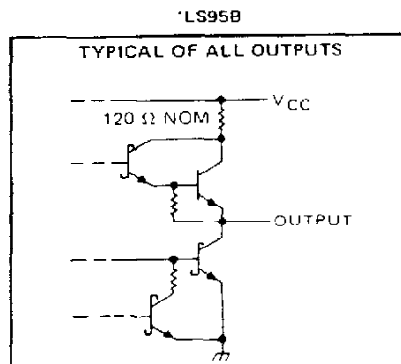
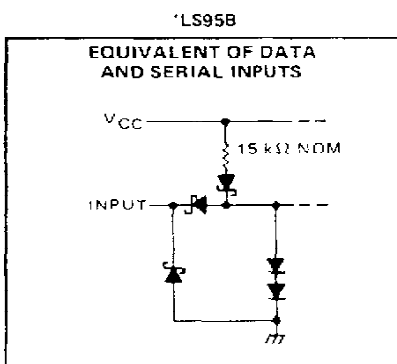
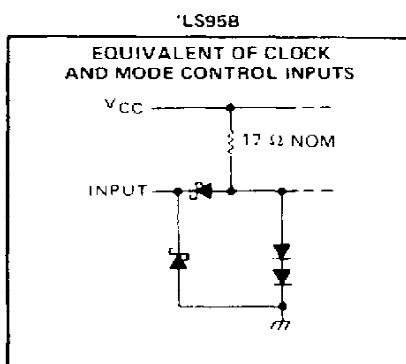
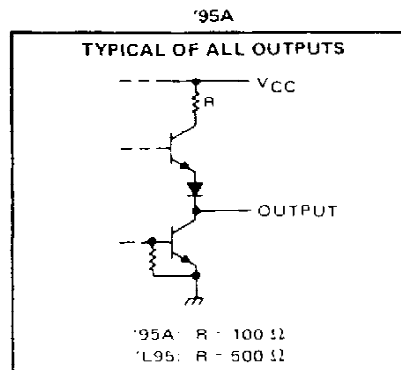
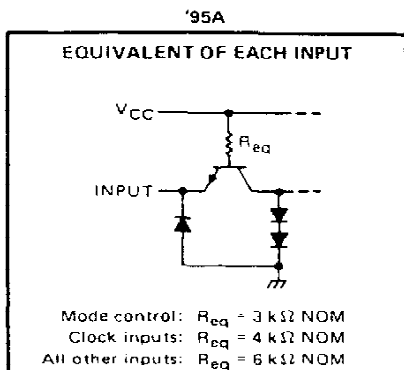


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SN5495A, SN54LS95B, SN7495A, SN74LS95G 4-BIT PARALLEL-ACCESS SHIFT REGISTERS

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	SN54'	SN54LS'	SN74'	SN74LS'	UNIT
Supply voltage, V_{CC} (see Note 1)	7	7	7	7	V
Input voltage	5.5	7	5.5	7	V
Interemitter voltage (see Note 2)	5.5		5.5		V
Operating free-air temperature range	-55 to 125		0 to 70		°C
Storage temperature range	-65 to 150		-65 to 150		°C

- NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
 2. This is the voltage between two emitters of a multiple-emitter input transistor. This rating applies between the clock-2 input and the mode control input of the '95A.

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SN5495A, SN7495A 4-BIT PARALLEL-SHIFT REGISTERS

recommended operating conditions

	SN5495A			SN7495A			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-800			-800	μ A
Low-level output current, I_{OL}			16			16	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock pulse, $t_{w(clock)}$ (See Figure 1)	20			20			ns
Setup time, high-level or low-level data, t_{SU} (See Figure 1)	15			15			ns
Hold time, high-level or low-level data, t_H (See Figure 1)	0			0			ns
Time to enable clock 1, $t_{enable 1}$ (See Figure 2)	15			15			ns
Time to enable clock 2 (See Figure 2)	15			15			ns
Time to inhibit clock 1, $t_{inhibit 1}$ (See Figure 2)	5			5			ns
Time to inhibit clock 2, $t_{inhibit 2}$ (See Figure 2)	5			5			ns
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS [†]	SN5495A			SN7495A			UNIT
			MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$			-1.5			-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OH} = -800 \mu\text{A}$	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2 \text{ V}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 16 \text{ mA}$		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			1			1	mA
I_{IH}	High-level input current	Serial, A, B, C, D, Clock 1 or 2			40			40	μ A
		Mode control			80			80	
I_{IL}	Low-level input current	Serial, A, B, C, D, Clock 1 or 2			-1.6			-1.6	mA
		Mode control			-3.2			-3.2	
I_{OS}	Short-circuit output current [§]	$V_{CC} = \text{MAX}$	-18		-57	-18		-57	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX}$, See Note 3		39	63		39	63	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

[§] Not more than one output should be shorted at a time.

NOTE 3: I_{CC} is measured with all outputs and serial input open; A, B, C, and D inputs grounded; mode control at 4.5 V; and a momentary 3 V, then ground, applied to both clock inputs.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	$C_L = 15 \text{ pF}$, $R_L = 400 \Omega$, See Figure 1	25	36		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from clock			18	27	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock			21	32	ns

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SN54LS95B, SN74LS95B

4-BIT PARALLEL-ACCESS SHIFT REGISTERS

recommended operating conditions

	SN54LS95B			SN74LS95B			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			4			8	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock pulse, $t_{w(clock)}$ (see Figure 1)	20			20			ns
Setup time, high-level or low-level data, t_{SU} (see Figure 1)	20			20			ns
Hold time, high-level or low-level data, t_H (see Figure 1)	20			10			ns
Time to enable clock 1, $t_{enable 1}$ (see Figure 2)	20			20			ns
Time to enable clock 2, $t_{enable 2}$ (see Figure 2)	20			20			ns
Time to inhibit clock 1, $t_{inhibit 1}$ (see Figure 2)	20			20			ns
Time to inhibit clock 2, $t_{inhibit 2}$ (see Figure 2)	20			20			ns
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS [†]	SN54LS95B			SN74LS95B			UNIT
		MIN	TYP [‡]	MAX	MIN	TYP [‡]	MAX	
V_{IH} High-level input voltage		2			2			V
V_{IL} Low-level input voltage				0.7			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} - V_{IL \text{ max}}, I_{OH} = -400 \mu\text{A}$	2.5	3.4		2.7	3.4		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} - V_{IL \text{ max}}, I_{OL} = 4 \text{ mA}$		0.25	0.4		0.25	0.4	V
						0.35	0.5	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}, V_I = 7 \text{ V}$			0.1			0.1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}, V_I = 2.7 \text{ V}$			20			20	μ A
I_{IL} Low-level input current	$V_{CC} = \text{MAX}, V_I = 0.4 \text{ V}$			-0.4			-0.4	mA
I_{OS} Short-circuit output current [§]	$V_{CC} = \text{MAX}$	-20		-100	-20		-100	mA
I_{CC} Supply current	$V_{CC} = \text{MAX},$ See Note 3		13	21		13	21	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

[‡] All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

[§] Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 3: I_{CC} is measured with all outputs and serial input open; A, B, C, and D inputs grounded; mode control at 4.5 V; and a momentary 3 V, then ground, applied to both clock inputs.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

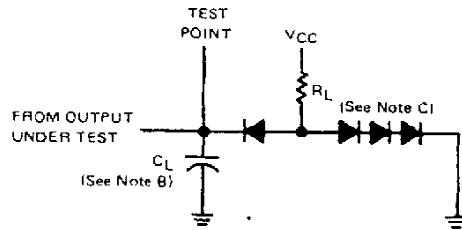
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max} Maximum clock frequency	$C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega,$ See Figure 1	25	36		MHz
t_{PLH} Propagation delay time, low-to-high-level output from clock			18	27	ns
t_{PHL} Propagation delay time, high-to-low-level output from clock			21	32	ns


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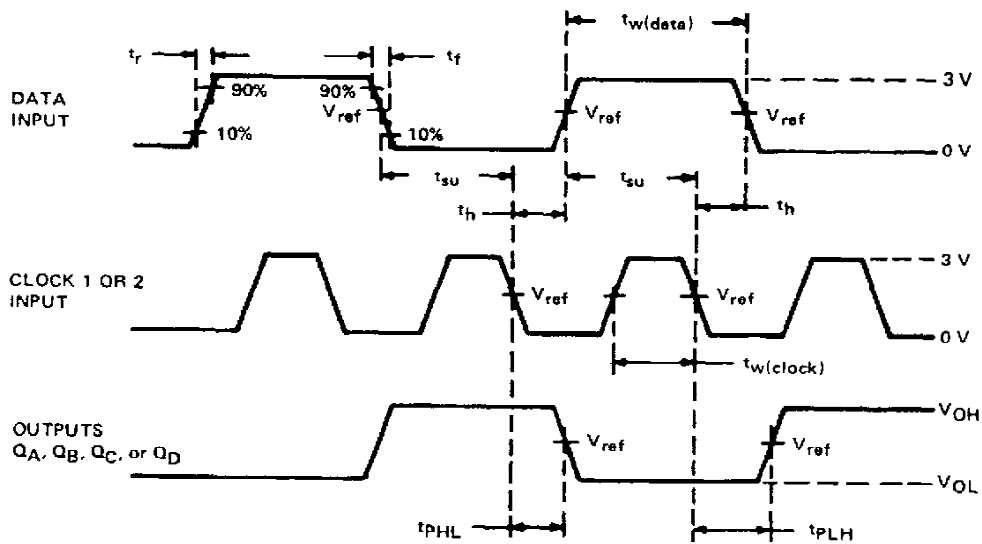
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SN5495A, SN54LS95B, SN7495A, SN74LS95B
4-BIT PARALLEL-ACCESS SHIFT REGISTERS

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT

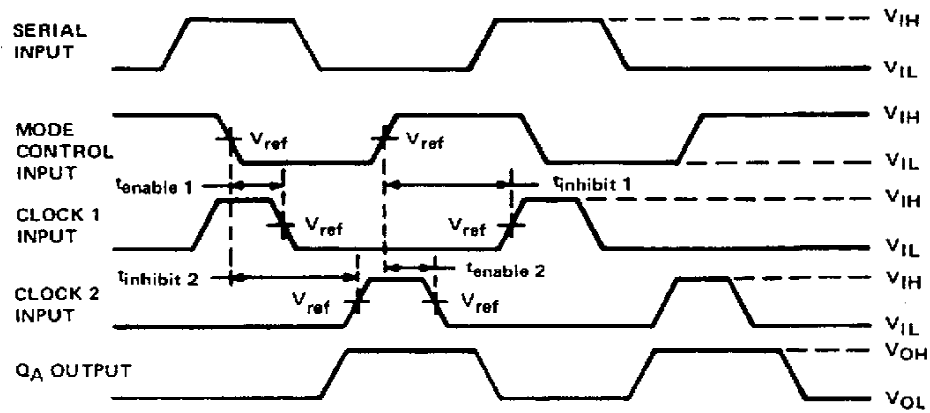


- NOTES: A. Input pulses are supplied by a generator having the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, and $Z_{out} \approx 50 \Omega$. For the data pulse generator, PRR = 500 kHz; for the clock pulse generator, PRR = 1 MHz. When testing f_{max} , vary PRR. For '95A, $t_w(data) \geq 20$ ns, $t_w(clock) \geq 15$ ns. For 'LS95B, $t_w(data) \geq 20$ ns, $t_w(clock) \geq 15$ ns.
- B. C_L includes probe and jig capacitance.
- C. All diodes are 1N3064 equivalent.
- D. For '95A, $V_{ref} = 1.5$ V; for 'LS95B, $V_{ref} = 1.3$ V.

VOLTAGE WAVEFORMS
FIGURE 1-SWITCHING TIMES

SN5495A, SN54LS95B, SN7495A, SN74LS95B
4-BIT PARALLEL-ACCESS SHIFT REGISTERS

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. Input is at a low level.
 B. For '95A, $V_{ref} = 1.5$ V; for 'LS95B, $V_{ref} = 1.3$ V.

VOLTAGE WAVEFORMS
FIGURE 2. CLOCK ENABLE/INHIBIT TIMES

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