

# **Configuring and Applying the MC74HC4046A Phase-Locked Loop**

A versatile device for 0.1 to 16MHz frequency synchronization

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# Configuring and Applying the MC74HC4046A Phase-Locked Loop

## A versatile device for 0.1 to 16MHz frequency synchronization

The MC74HC4046A (hereafter designated HC4046A) phase-locked loop contains three phase comparators, a voltage-controlled oscillator (VCO) and an output amplifier. The user of this document should have a copy of the HC4046A data sheet in Motorola Data Book DL129 available for details of device operation and operating specifications. The user should also be aware that the following information is useful

for approximating a design **but**, because of process, layout and other variables, there can be substantial deviation between theory and actual results. Therefore, **it is highly recommended that prototypes be built and checked before committing a design to production.**

Typical applications for the HC4046A usually involve a configuration such as shown in Figure 1.

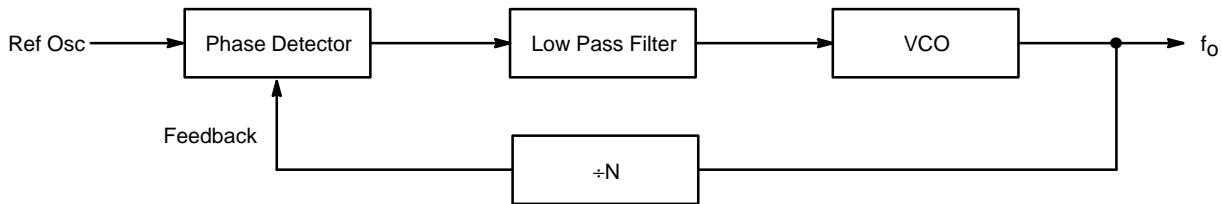


Figure 1. Typical Phase-Locked Loop

### VCO/OUTPUT FREQUENCY

The output frequency,  $F_o$ , is calculated as a function of the Ref Osc input and the  $\div N$  feedback counter:

$$F_o = \text{Ref Osc} * N \quad (1)$$

The ability of the loop to emulate the above formula makes it ideal for multiplying an input frequency by any number up to the maximum of the VCO. The HC4046A VCO frequency is controlled by the equation:

$$\text{VCO freq} = f(I * C) \quad (2)$$

where  $I$  is controlled by the external resistors  $R_1$  and  $R_2$  and  $C$  by external capacitor  $C_{ext}$ .

Frequency of oscillation is calculated by starting with the familiar equation:

$$I = c \frac{dV}{dt} \quad (3)$$

and reworking it to obtain a formula that incorporates all the detail to fit the HC4046A. First, the charge time of the device for half-cycle time is obtained as follows:

$$dt = dV \frac{C}{I} \quad \text{and} \quad F_o = \frac{1}{2dt}$$

$$\text{or, } F_o = \frac{1}{2CdV} = \frac{I}{2CdV} \quad (4)$$

where  $I$  and  $dV$  must be obtained for the HC4046A.

There are two components that comprise the  $I$  charge for the HC4046A VCO,  $I_1$  and  $I_2$ .  $I_1$  is the current that sets the frequency associated with the VCO input and is a function of  $R_1$ ,  $VCO_{in}$ , and an internal current mirror that is ratioed at  $120/5 \approx 24$ , resulting in the equation:

$$I_1 = \frac{VCO_{in}}{R_1} \left( \frac{120}{5} \right) \quad (5)$$

$I_2$  is set by  $R_2$  and adds a constant current to limit the  $F_o$  min of the VCO and is a function of  $V_{dd}$ ,  $R_2$ , and an internal current mirror of ratio  $23/5$ , resulting in the equation:

$$I_2 = \left( \frac{2V_{dd}}{3R_2} \right) \left( \frac{23}{5} \right) \quad (6)$$

The  $dV$  of Equation (4) is determined by design to be  $\approx 1/3 V_{dd}$ . Substituting this and  $I = I_1 + I_2$  into Equation (4) results in:

$$\begin{aligned} F_o &= \frac{\frac{VCO_{in}}{R_1} \left( \frac{120}{5} \right) + \left( \frac{2V_{dd}}{3R_2} \right) \left( \frac{23}{5} \right)}{2C_{ext} \frac{V_{dd}}{3}} \\ &= \frac{\frac{VCO_{in}}{R_1} (24) + \left( \frac{2V_{dd}}{3R_2} \right) (4.6)}{2C_{ext} \frac{V_{dd}}{3}} \quad (4.6) \\ &= \frac{3VCO_{in} (24) + \frac{2V_{dd}}{R_2} (4.6)}{2C_{ext} V_{dd}} \quad (7) \end{aligned}$$

It was found by experiment that when the  $C_{ext}$  potential reaches threshold (at  $V_{dd}/3$ ), the inversion of the charging voltage of  $C_{ext}$  is forced below ground due to charge coupling. Therefore, the  $dV$  is not just  $V_{dd}/3$  as expected and the charg-

ing time must start at a point below ground which affects  $t$  and thus,  $F_O$ . An undershoot voltage must be added to the equation for better accuracy in calculating  $t$  and  $F_O$ . This modifies Equation ( 7 ) as follows:

$$F_O = \frac{\frac{3V_{COin}}{R_1} (24) + \frac{2V_{dd}}{R_2} (4.6)}{2C_{ext} (V_{dd} + 3 * \text{undershoot})}$$

$$= \frac{\frac{3V_{COin}(I_{constant \text{ ratio}})}{R_1} + \frac{9.2(V_{dd})}{R_2}}{2C_{ext} (V_{dd} + 3 * \text{undershoot})} \quad (8)$$

Equation ( 8 ) now contains all the factors to calculate an  $F_O$  for the HC4046A VCO.

It was determined by experiment that the undershoot of the charging waveform is a function of  $C_{ext}$  and an on-chip parasitic diode that clamps it at a maximum of  $-0.7V$ . The size of the  $C_{ext}$  capacitor limits the voltage and was found to be near zero volts for  $C_{stray} \approx 17pF \leq C_{ext} \leq 30pF$ ; the voltage increases at  $6 \text{ mV/pF}$  for a  $30pF \leq C_{ext} \leq 150pF$  range of  $C_{ext}$ . The on-chip diode then takes over and limits the voltage to  $-0.7V$ .

It was also found that the  $I_{constant \text{ ratio}}$  is a function of  $R_1$  and increases as  $R_1$  becomes larger. The change is attributed to saturation of the current mirror at lower value resistances, and to voltage divider problems at higher value resistances combined with the resistance of the small FET in the current mirror. Experimental data shows that  $I_{constant \text{ ratio}}$  follows Table 1 somewhat. The ratio goes to 25 somewhere between  $9.1K\Omega$  and  $51K\Omega$ , and for those limits, 25 should give reasonable results. In addition, these numbers seem to hold for a range of  $V_{dd}$  of  $3.0V \leq V_{dd} \leq 6V$ .

**Table 1.  $I_{constant \text{ ratio}}$  versus  $R_1$**

$R_1$ (K $\Omega$ )	$I_{constant \text{ ratio}}$
3.0	13.5
5.1	17.5
9.1	21.5
12	23.0
15	24.0
30	26.5
40	27.0
51	28.5
110	29.0
300	31.0

The VCO calculation [Equation ( 8 )] becomes a bit more accurate by adjusting the  $V_{COin}$  and  $I_{constant \text{ ratio}}$ . For example, with  $R_1 = 300K$ ,  $R_2 = \infty$ ,  $C_{ext} = 0.1\mu F$ ,  $V_{COin} = 1.0V$ ,  $V_{dd} = 4.5V$ , and  $I_{constant \text{ ratio}} = 31$ , Equation ( 8 ) yields:

$$F_O = \frac{\frac{(3)(1)(31)}{300K}}{2(0.1 * 10^{-6})(4.5 + 2.1)}$$

$$= 235\text{Hz}$$

For comparison, from Chart 14D in the HC4046A data sheet, the  $F_O$  based on measurements is approximately 270 Hz. Thus, the calculated and measured values are not too far apart taking into consideration such variables as process variation, temperature, and breadboard inaccuracies. The  $C_{stray}$

of a PCB layout will affect results if the  $C_{ext}$  is not  $\gg C_{stray}$ . So for  $C_{ext} \leq 1000pF$ , adding  $C_{stray}$  to the  $C_{ext}$  fixed capacitance will result in better accuracy.

The gain of a VCO is calculated by knowing  $f_{max}$  at  $V_{COin \text{ max}}$  and  $f_{min}$  at  $V_{COin \text{ min}}$  and calculating the following equation:

$$VCO \text{ gain} = \frac{f_{max} - f_{min}}{V_{COin \text{ max}} - V_{COin \text{ min}}} \quad (9)$$

$$= \Delta \text{freq/volt}$$

The gain of the VCO is needed to calculate a suitable loop filter for a PLL system.

$F_O$  is determined by  $V_{COin}$  and is clamped as a function of a % of  $V_{dd}$ . The clamp voltage generally follows the slope of  $4\%/V$  for  $V_{dd}$  changes from  $3.5V \leq V_{dd} \leq 6V$ , starting at  $56\%$  at  $V_{dd} = 3.5V$  and going to  $66\%$  at  $V_{dd} = 6V$ . Knowing this limit point allows picking a  $V_{COin \text{ max}}$  point a few hundred mV below it and keeps  $F_O$  in the linear range of operation. It also best to pick a  $V_{COin \text{ min}}$  point at a level of a few hundred mV above  $0V$  for the same reason given above.

As an example, for a  $C_{ext} = 1100pF$ ,  $R_1 = 9.1K$ ,  $R_2 = \infty$ ,  $V_{dd} = 5.0V$ , and  $V_{COin \text{ min}} = 0.25V$ ,  $V_{COin \text{ max}}$  can be determined and a gain calculated as follows.  $V_{COin \text{ limit}} = (4\%/V)(1.5V) + 56\% = (62\%)(V_{dd}) = 3.1V$ . So, for sake of linearity, choose  $V_{COin} = 2.5V$ . Using Equation ( 8 ),  $V_{COin \text{ min}}$  and  $V_{COin \text{ max}}$  can be used to calculate  $F_O \text{ min}$  and  $F_O \text{ max}$  as follows:

$$F_O \text{ min} = \frac{\frac{(3)(0.25)(21.5)}{9.1K}}{2(1100 * 10^{-12})(5 + 2.1)} = 113.4\text{KHz}$$

$$F_O \text{ max} = \frac{\frac{(3)(2.5)(21.5)}{9.1K}}{2(1100 * 10^{-12})(5 + 2.1)} = 1.3\text{MHz}$$

Then, using Equation ( 9 ), the VCO gain is:

$$VCO \text{ gain} = \frac{1.3 * 10^6 - 0.11 * 10^6}{2.5 - 0.25} = 528.9\text{KHz/V}$$

This gain factor will be known as  $K_{VCO}$  in the loop filter equations.

$R_2$  is used in applications where a minimum output frequency is desired when  $V_{COin}$  is  $0V$ . It is calculated at  $V_{COin} = 0V$  causing Equation ( 8 ) to become:

$$F_O = \frac{9.2 (V_{dd})}{2C (R_2) (V_{dd} + 3 * \text{undershoot})}$$

The additional  $I_2$  current is a constant that adds to total charge current for  $C_{ext}$  and increases the  $V_{COin}$  versus  $F_O$  curve by a theoretical constant amount. In reality, the amount of increase actually decreases at a slight rate as  $V_{COin}$  increases. The decrease is slight and the use of Equation ( 8 ) will give adequate accuracy for most applications.

The  $F_{max}$  of the HC4046A VCO was determined to be about 16MHz. Beyond 16MHz, the output logic swing tends to reduce and is therefore somewhat useless for driving a CMOS input. The VCO will operate at  $\approx 28\text{MHz}$  but the output has a  $V_{OL} \approx 2.0V$  and a  $V_{OH} \approx 4.5V$  at  $V_{dd} = 5.0V$ .

The following table was generated to make calculation of  $R_1$  and  $C_{ext}$  a function of  $F_0$  with  $V_{dd} = 5V$ ,  $VCO_{in} = 1V$ , and room temperature. Use of the table allows a rough estimate of  $(R_1)(C_{ext})$  for a given  $F_0$ . The final values can be adjusted by use of Equation ( 8 ), Table 1 for  $I_{constant}$  ratio, rules for undershoot voltage,  $V_{dd}$  variations, and  $VCO_{in}$  variations. The example below shows a typical calculation.

**Table 2.  $(R_1)(C_{ext})$  versus  $F_0$**

$R_1$ ( $\Omega$ )	$C_{ext}$ (pF)	$(R_1)(C_{ext})$
$3.0K \leq R_1 \leq 9.0K$	$0 \leq C_{ext} \leq 30$	$5.40/F_0$
	$30 \leq C_{ext} \leq 150$	$4.15/F_0$
	$150 \leq C_{ext} \leq \infty$	$3.80/F_0$
$9.1K \leq R_1 \leq 50K$	$0 \leq C_{ext} \leq 30$	$7.50/F_0$
	$30 \leq C_{ext} \leq 150$	$5.77/F_0$
	$150 \leq C_{ext} \leq \infty$	$5.28/F_0$
$50K \leq R_1 \leq 900K$	$0 \leq C_{ext} \leq 30$	$9.00/F_0$
	$30 \leq C_{ext} \leq 150$	$6.92/F_0$
	$150 \leq C_{ext} \leq \infty$	$6.34/F_0$

Assume a desired value of  $F_0$  of 1MHz. From Table 2, choose an  $R_1$  range of  $9.1K \leq R_1 \leq 50K$  and a  $C_{ext}$  range of  $> 150pF$ ; this condition leads to  $(R_1)(C_{ext}) = 5.28/F_0$ . Thus,

$$(R_1) (C_{ext}) = \frac{5.28}{1 * 10^6} = 5.28 * 10^{-6}$$

Now choose a  $C_{ext}$  of 200pF. Then, from above result,

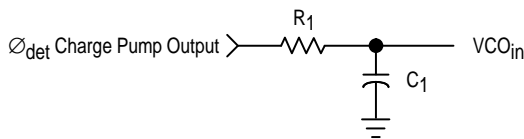
$$R_1 = \frac{5.28 * 10^{-6}}{200 * 10^{-12}} = 26K$$

This appears reasonable and there are standard values for  $C_{ext} = 200pF$  and  $R_1 = 27K$ . Using these values, Equation ( 8 ) can be adjusted according to the desired  $F_0$  min,  $F_0$  max, and  $F_0$  center.

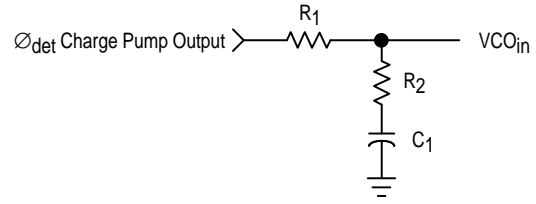
**LOW PASS FILTER DESIGN**

The design of low pass filters is well known and the intent here is to simply show some typical examples. Reference should be made to the HC4046A Data Sheet and to Motorola Application Note AN535/D — “Phase-Locked Loop Fundamentals” (available through Motorola Literature Distribution).

Some simple types of low pass filters are shown in Figure 2 and Figure 3.



**Figure 2. Simple Low Pass Filter A**



**Figure 3. Simple Low Pass Filter B**

The equations for calculating loop natural frequency ( $\omega_n$ ) and damping factor ( $d$ ) are as follows:

For Filter A (Figure 2):

$$\omega_n = \sqrt{\frac{K_{\phi}K_{VCO}}{NC_1R_1}}$$

$$d = \frac{0.5\omega_n}{K_{\phi}K_{VCO}}$$

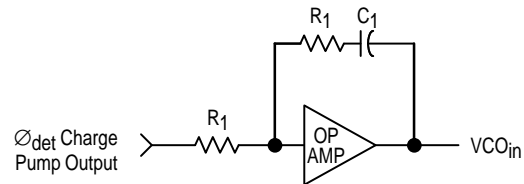
where  $K_{\phi}$  = phase detector gain,  $K_{VCO}$  = VCO gain, and  $N$  = divide counter.

For Filter B (Figure 3):

$$\omega_n = \sqrt{\frac{K_{\phi}K_{VCO}}{NC_1(R_1 + R_2)}}$$

$$d = 0.5\omega_n(R_2C_1 + \frac{N}{K_{\phi}K_{VCO}}) \tag{10}$$

Figure 4 shows an active filter using an op amp from Application Note AN535/D.



**Figure 4. Op Amp Filter**

For Figure 4, the equations become:

$$\omega_n = \sqrt{\frac{K_{\phi}K_{VCO}}{NC_1R_1}} \tag{11}$$

$$d = \frac{K_{\phi}K_{VCO}R_2}{2\omega_nNR_1} \tag{12}$$

$$= \frac{\omega_nC_1R_2}{2}, \text{ where Op Amp gain is large}$$

From the above equations, it is possible to design a suitable filter to meet the needs of many PLL applications. The inclusion of  $R_2$  in the equations for Figure 3 and Figure 4 permits the capability to change  $\omega_n$  and  $d$  separately while Figure 2

equations do not. Normally, a design is easier if  $w_n$  and  $d$  can be chosen independently. Both factors affect the loop acquisition time and stability. A good starting value for  $d$  is  $F_{ref}/10$  for  $w_n$ .

Manipulation of the equations allows calculation of  $R_1$ ,  $R_2$ , and  $C_1$  from the other measured, calculated, or picked parameters. For example,

$$R_1 + R_2 = \frac{K_{\phi} K_{VCO}}{N C_1 w_n^2} \quad (13)$$

$$R_2 = \frac{2d}{C_1 w_n} - \frac{N}{C_1 (K_{\phi} K_{VCO})} \quad (14)$$

$$C_1 = \frac{K_{\phi} K_{VCO}}{N w_n^2 (R_1 + R_2)}, \text{ or alternatively,}$$

$$C_1 = \frac{2d}{R_2 w_n} - \frac{N}{R_2 (K_{\phi} K_{VCO})}$$

Usually,  $C_1$ ,  $w_n$ , and  $d$  are picked and the remaining parameters calculated.

## DESIGN EXAMPLE

The goal is to design a phase-locked loop that has an  $F_{ref}$  of 100KHz, an output  $F_o$  of 1MHz center frequency, and the ability to move from 200KHz to 2MHz in 100KHz steps.

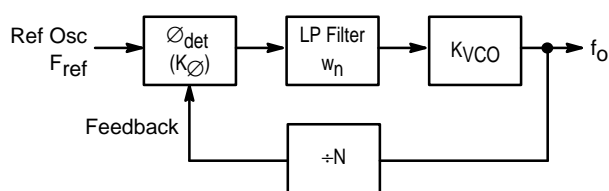


Figure 5. Parametized PLL

To determine  $N$ , use equation (1) for  $F_o \text{ min} = 200\text{KHz}$ , and  $F_o \text{ max} = 2\text{MHz}$  resulting in the following:

$$N \text{ min} = 200/100 = 2, \text{ and}$$

$$N \text{ max} = 2000/100 = 20$$

The results so far indicate the following starting parameters:

A. A VCO with a 10:1 range is required

B.  $w_n = F_{ref}/10 = 10\text{KHz}$

C.  $d = 0.707$

D.  $R_2 = \infty$

E.  $V_{dd} = 5.0\text{V}$

The  $F_o$  center frequency  $\approx$

$$\frac{F_{\text{max}} + F_{\text{min}}}{2} = \frac{2.0 + 0.2}{2} = 1.1\text{MHz}$$

Recalling that the clamp voltage % at  $V_{dd} = 5\text{V}$  is about 62, then  $F_{\text{max}} \text{ VCO}_{in} \text{ limit} = (0.62)(5) = 3.1\text{V}$ , but as described earlier, this needs to be reduced by a factor to bring it into linearity ( $\approx 350\text{mV}$ ) so the final  $F_{\text{max}} \text{ VCO}_{in} \text{ limit} = 2.75\text{V}$ .

For the  $F_{\text{min}} \text{ VCO}_{in}$  limit pick  $0.25\text{V}$ . This results in a center frequency  $\text{VCO}_{in}$  of:

$$\text{Center freq } \text{VCO}_{in} = \frac{2.75 - 0.25}{2} = 1.25\text{V}$$

From Table 2, for picked values of  $9.1\text{K} \leq R_1 \leq 50\text{K}$  and  $30 \leq C_{\text{ext}} \leq 150$ , obtain an estimate for  $(R_1)(C_{\text{ext}})$  of  $5.77/F_o$ . Thus, at the  $F_o$  center frequency,

$$(R_1)(C_{\text{ext}}) = \frac{5.77}{1.1 * 10^6} = 5.245 * 10^{-6}$$

Now, a reasonable starting point is established for setting the values of the loop filter and the VCO range. Choosing  $R_1 = 9.1\text{K}$ ,  $C_{\text{ext}}$  becomes

$$C_{\text{ext}} = \frac{5.245 * 10^{-6}}{9.1\text{K}} = 576\text{pF WHOOPS!}$$

This value,  $576\text{pF}$ , is outside of the original picked range for  $C_{\text{ext}}$ ; therefore, we need to go back and pick a larger value of  $R_1$ , e.g.,  $42\text{K}$  should be sufficient. Then  $C_{\text{ext}}$  becomes

$$C_{\text{ext}} = \frac{5.245 * 10^{-6}}{42\text{K}} = 125\text{pF}$$

and now both  $R_1$  and  $C_{\text{ext}}$  are within selected ranges.

Now calculate  $F_{\text{max}}$  and  $F_{\text{min}}$  using Equation (8) with  $R_1 = 42\text{k}\Omega$ ,  $R_2 = \infty$ ,  $V_{dd} = 5.0\text{V}$ ,  $I_{\text{constant}} = 27$  (from Table 1. and  $R_1 = 42\text{k}\Omega$ ),  $V_{\text{undershoot}} = 0.57\text{V}$  (calculated from  $6\text{pF/mV}$  ( $125\text{pF} - 30\text{pF}$ ) =  $0.57\text{V}$ ),  $\text{VCO}_{in} \text{ min} = 0.25\text{V}$ , and  $\text{VCO}_{in} \text{ max} = 2.75\text{V}$ :

$$F_o \text{ min} = \frac{\frac{(3)(0.25)(27)}{42\text{K}} + \frac{(9.2)(5.0)}{\infty}}{(2)(125 * 10^{-12}\text{f}) [5.0\text{V} + 3(0.57\text{V})]}$$

$$= \frac{20.25}{70.455 * 10^{-6}} = 287.4\text{KHz}$$

$$F_o \text{ max} = \frac{\frac{(3)(2.75)(27)}{42\text{K}} + \frac{(9.2)(5.0)}{\infty}}{(2)(125 * 10^{-12}\text{f}) [5.0\text{V} + 3(0.57\text{V})]}$$

$$= \frac{222.75}{70.455 * 10^{-6}} = 3.16\text{MHz}$$

$F_{\text{max}}$  is  $>$  the required  $2.0\text{MHz}$ , but the  $F_{\text{min}}$  is not low enough for required application. It is necessary to adjust either  $C_{\text{ext}}$  or  $R_1$  to achieve required specification of  $0.2$  to  $2.0\text{MHz}$   $F_o$ . Since  $R_1 = 42\text{k}\Omega$  is a standard resistor value, try adjusting  $C_{\text{ext}}$  to a higher value, such as  $175\text{pF}$ . Because  $C_{\text{ext}}$  is now  $>$   $150\text{pF}$ , the  $V_{\text{undershoot}}$  must be adjusted to  $0.7\text{V}$ , as per earlier explanation:

# AN1410

So,

$$F_{O \min} = \frac{\frac{(3)(0.25)(27)}{42K} + \frac{(9.2)(5.0)}{\infty}}{(2)(175 * 10^{-12}f) [5.0V + 3(0.7V)]}$$

$$= \frac{20.25}{104.37 * 10^{-6}} = 194.02\text{KHz}$$

and

$$F_{O \max} = \frac{\frac{(3)(2.75)(27)}{42K} + \frac{(9.2)(5.0)}{\infty}}{(2)(175 * 10^{-12}f) [5.0V + 3(0.7V)]}$$

$$= \frac{222.75}{104.37 * 10^{-6}} = 2.13\text{MHz}$$

These values are adequate for the specified application.

The next item to determine is the VCO gain factor,  $K_{VCO}$ , using Equation ( 9 ):

$$K_{VCO} = \frac{f_{\max} - f_{\min}}{VCO_{in \max} - VCO_{in \min}}$$

$$K_{VCO} = \frac{2.13 * 10^6 - 0.194 * 10^6}{2.75V - 0.25V} = 774.4\text{KHz/V}$$

or in radians

$$= (2\pi) (774.4 * 10^3) = 4.86 * 10^6\text{Rad/sec/V}$$

The final values used for the desired frequency range are  $R_1 = 42k\Omega$ ,  $C_{ext} = 175pF$ ,  $R_2 = \infty$ ,  $VCO_{in \max} = 2.75V$ , and  $VCO_{in \min} = 0.25V$ .

The next step is to determine the loop filter. Choosing a filter like the one in Figure 3, calculate the component as follows:

$$K_{\phi} = \frac{V_{dd}}{4\pi} = \frac{5.0}{4\pi} = 0.4V/\text{rad}$$

$$w_n = \frac{100\text{KHz}}{10} = 10\text{KHz} * 2\pi = 62.83 * 10^3\text{rad/sec}$$

$d = 0.707$  (for starters), and

$N = 2$  to  $20$

where

$K_{\phi}$  = phase detector gain

$V_{dd}$  = output swing

Choose  $C_1$  to be  $0.01\mu F$ ,  $N = 10$  for approximate mid-range  $F_o$ , and calculate  $R_1$  and  $R_2$  using Equations ( 13 ) and ( 14 ):

$$R_1 + R_2 = \frac{K_{\phi}K_{VCO}}{NC_1w_n^2} = \frac{(0.4)(4.86 * 10^6)}{(10)(0.01 * 10^{-6})(62.83 * 10^3)^2}$$

$$= \frac{1.944 * 10^6}{394.76} = 4924.5\Omega$$

$$R_2 = \frac{2d}{C_1w_n} - \frac{N}{C_1(K_{\phi}K_{VCO})}$$

$$= \frac{(2)(0.707)}{(0.01 * 10^{-6})(62830)} - \frac{10}{(0.01 * 10^{-6})(0.4)(4.86 * 10^6)}$$

$$= 2250.52 - 514.4 = 1736\Omega$$

Then,  $R_1 = 4924.5 - 1736 = 3188.5\Omega$ .

Since  $N$  is changeable, it is a good idea to check min and max on  $w_n$  and  $d$ . For more information on why, see Motorola Application Note AN535/D or the MC4044 Data Sheet in the MECL Data Book DL122/D. The following examples show sample calculations for  $N = 2$  and  $20$ .

For  $N = 20$ , use Equation ( 10 ) to calculate  $w_n$  and  $d$ :

$$w_n \min = \sqrt{\frac{K_{\phi}K_{VCO}}{NC_1(R_1 + R_2)}}$$

$$= \sqrt{\frac{(0.4)(4.86 * 10^6)}{(20)(0.01 * 10^{-6})(3188.5 + 1736)}}$$

$$= 44.43 * 10^3\text{rad/sec, or}$$

$$= \frac{44.43 * 10^3\text{rad/sec}}{2\pi} \approx 7\text{KHz}$$

and

$$d \min = (0.5)(w_n) \left[ R_2C_1 + \frac{N}{K_{\phi}K_{VCO}} \right]$$

$$= (0.5)(44.43 * 10^3) * \left[ (1736)(0.01 * 10^{-6}) + \frac{20}{(0.4)(4.86 * 10^6)} \right]$$

$$= 0.6144$$

For N = 2:

$$\begin{aligned} \omega_n \max &= \sqrt{\frac{(0.4)(4.86 * 10^6)}{(2)(0.01 * 10^{-6})(3188.5 + 1736)}} \\ &= 140.49 * 10^3 \text{rad/sec, or} \\ &= \frac{140.49 * 10^3 \text{rad/sec}}{2\pi} = 22.36 \text{KHz} \end{aligned}$$

and


$$\begin{aligned} d_{\max} &= (0.5)(140.49 * 10^3) * \\ &\quad \left[ (1736)(0.01 * 10^{-6}) + \frac{2}{(0.4)(4.86 * 10^6)} \right] \\ &= 1.292 \end{aligned}$$

This shows the effect of changing n on loop performance and for this application is adequate.

If the components are not what is desired, choosing a different  $\omega_n$  and/or d allows them to be modified.

Alternatively, picking different C, R<sub>1</sub> or R<sub>2</sub> and recalculating the other parameters can be done. If the filter does not provide adequate performance, making  $\omega_n$  smaller or d larger may improve stability.

Note: Application Note AN535/D can also be found in BR1334/D, Motorola's High Performance Frequency Control Products book, also available through the literature distribution center.

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