

Product Specifications

Features

- Fully Field-Programmable:
 - I/O functions
 - Digital logic functions
 - Interconnections
- General-purpose array architecture
- Complete user control of design cycle
- Compatible arrays with logic cell complexity equivalent from 600 to 1,500 gates
- Standard product availability
- 100% factory-tested
- Selectable configuration modes
- Low-power, CMOS, static-memory technology
- Performance equivalent to TTL SSI/MSI
- TTL or CMOS input thresholds
- Complete development system support
 - XACT Design Editor
 - Schematic Entry
 - Macro Library
 - Timing Calculator
 - Logic and Timing Simulator
 - Auto Place/Route

Description

The Logic Cell Array (LCA) is a high density CMOS integrated circuit. Its user-programmable array architecture is made up of three types of configurable elements: Input/Output Blocks, logic blocks and Interconnect. The designer can define individual I/O blocks for interface to external circuitry, define logic blocks to implement logic functions and define interconnection networks to compose larger scale logic functions. The XACT Development System provides interactive graphic design capture and automatic routing. Both logic simulation and in-circuit emulation are available for design verification.

The Logic Cell Array is available in a variety of logic capacities, package styles, temperature ranges and speed grades.

Device	Logic Capacity (gates)	CLBs	User I/O Max	Config. bits
XC2064	600 - 1,000	64	58	12038
XC2018	1,000 - 1,500	100	74	17878

The LCA logic functions and interconnections are determined by data stored in internal static-memory cells. On-chip logic provides for automatic loading of configuration data at power-up. The program data can reside in an EEPROM, EPROM or ROM on the circuit board or on a floppy disk or hard disk. The program can be loaded in a number of modes to accommodate various system requirements.

Xilinx maintains test specifications for each product as controlled documents. To insure the use of the most recently released device performance parameters, please request a copy of the current test-specification revision.

Absolute Maximum Ratings

Symbol	Description		Units
V _{CC}	Supply voltage relative to GND	−0.5 to +7.0	V
V _{IN}	Input voltage with respect to GND	−0.5 to V _{CC} +0.5	V
V _{TS}	Voltage applied to 3-state output	−0.5 to V _{CC} +0.5	V
T _{STG}	Storage temperature (ambient)	−65 to +150	°C
T _{SOL}	Maximum soldering temperature (10 s @ 1/16 in.)	+260	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Operating Conditions

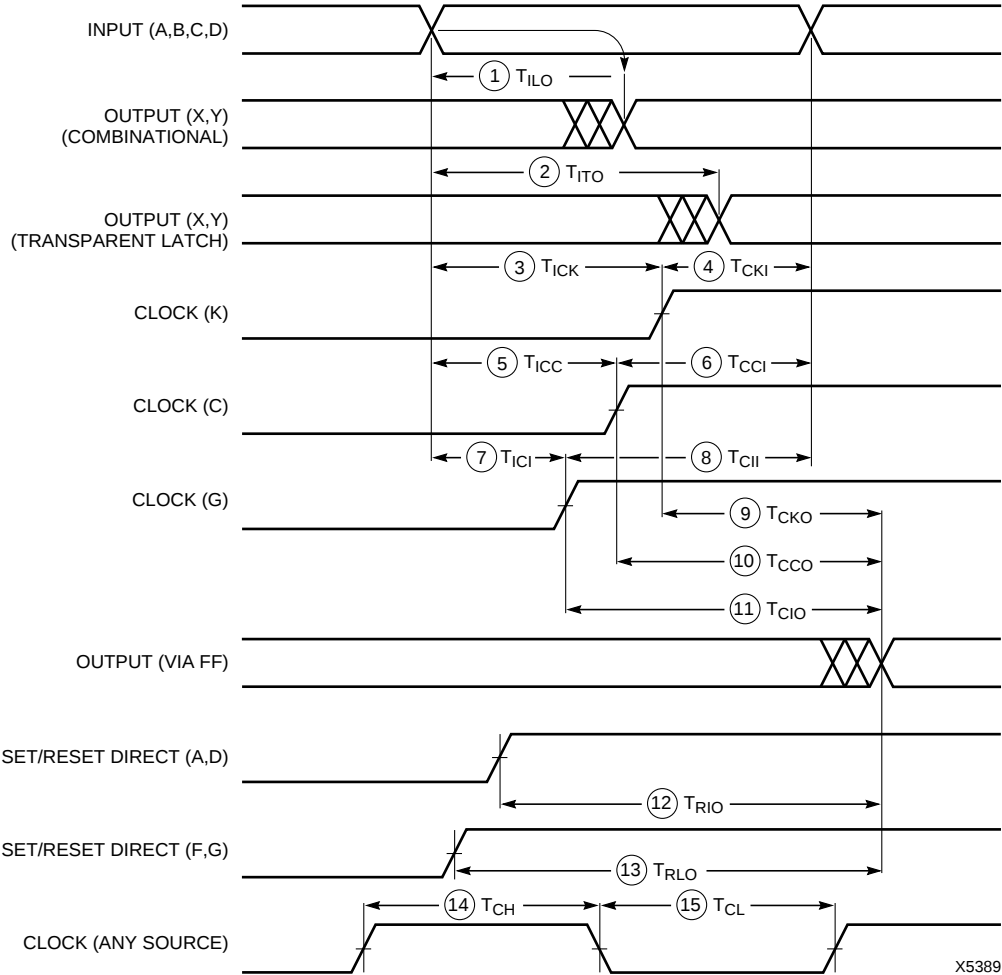
Symbol	Description	Min	Max	Units
V _{CC}	VCC relative to GND Commercial 0°C to +85°C junction	4.75	5.25	V
	VCC relative to GND Industrial −40°C to +100°C junction	4.5	5.5	V
	VCC relative to GND Military −55°C to +125°C case	4.5	5.5	V
V _{IHT}	High-level input voltage — TTL configuration	2.0	V _{CC}	V
V _{ILT}	Low-level input voltage — TTL configuration	0	0.8	V
V _{IHC}	High-level input voltage — CMOS configuration	70%	100%	V _{CC}
V _{ILC}	Low-level input voltage — CMOS configuration	0	20%	V _{CC}
T _{IN}	Input signal transition time		250	ns

At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.3% per °C.

DC Characteristics Over Operating Conditions

Symbol	Description		Min	Max	Units
V_{OH}	High-level output voltage (@ $I_{OH} = -4.0$ ma V_{CC} min)	Commercial	3.86		V
V_{OL}	Low-level output voltage (@ $I_{OL} = 4.0$ ma V_{CC} min)			0.32	V
V_{OH}	High-level output voltage (@ $I_{OH} = -4.0$ ma V_{CC} min)	Industrial Military	3.76		V
V_{OL}	Low-level output voltage (@ $I_{OL} = 4.0$ ma V_{CC} min)			0.37	V
V_{CCPD}	Power-down supply voltage (<u>PWRDWN</u> must be Low)		2.3		V
I_{CCO}	Quiescent operating power supply current				
	CMOS thresholds (@ V_{CC} Max)			5	mA
	TTL thresholds (@ V_{CC} Max)			12	mA
I_{CCPD}	Power-down supply current ($V_{CC(MAX)}$ @ T_{MAX})			500	μ A
I_{IL}	Input Leakage Current		-10	+10	μ A
C_{IN}	Input capacitance (sample tested) All Pins except XTL1 and XTL2 XTL1 and XTL2			10 15	pF pF

CLB Switching Characteristic Guidelines



X5389

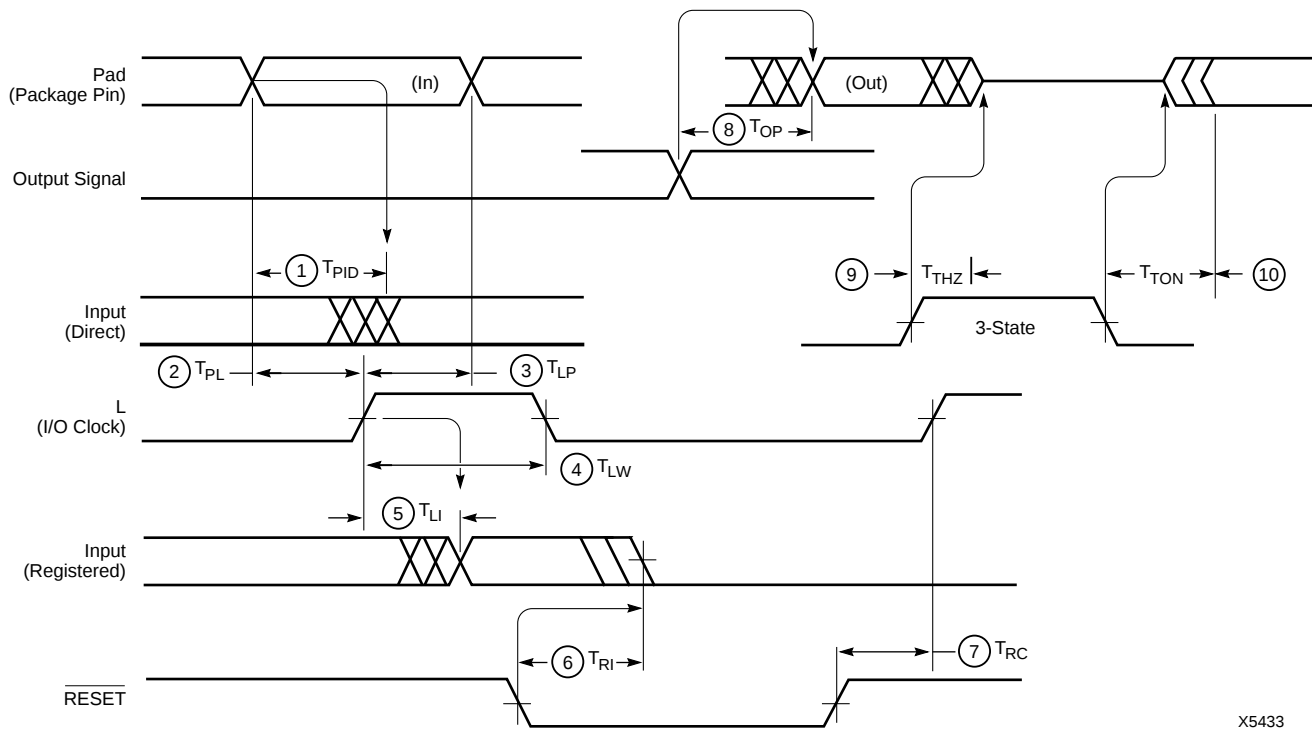
CLB Switching Characteristic Guidelines (Continued)

Speed Grade				-70		-100		-130		Units
	Description	Symbol		Min	Max	Min	Max	Min	Max	
Logic Input to Output	Combinatorial Transparent latch Additional for Q through F or G to out	1	T_{ILO}		10		8		5.5	ns
		2	T_{ITO}		14		10		8	ns
			T_{QLO}		6		6		3.7	ns
K Clock	To output Logic-input setup Logic-input hold	9	T_{CKO}		10		7		7	ns
		3	T_{ICK}	7		6		2.5		ns
		4	T_{CKI}	0		0		1.0		ns
C Clock	To output Logic-input setup Logic-input hold	10	T_{CCO}		13	9			7	ns
		5	T_{ICC}	6		5		3		ns
		6	T_{CCI}	0		0		1		ns
Logic Input to G Clock	To output Logic-input setup Logic-input hold	11	T_{CIO}		20		13		13	ns
		7	T_{ICI}	3		2		0		ns
		8	T_{CII}	4		3		5		ns
Set/Reset direct	Input A or D to output x, y Through F or G to output Reset pad to output x, y Separation of set/reset Set/Reset pulse-width	12	T_{RIO}		16		10		8	ns
		13	T_{RLO}		21		14		11	ns
			T_{MRQ}		20		17		13	ns
			T_{RS}	7		6		5		ns
			T_{RPW}	7		6		5		ns
Flip-flop Toggle rate	Q through F to flip-flop		F_{CLK}	70		*100		130		MHz
Clock	Clock High	14	T_{CH}	7		*5		3.5		ns
	Clock Low	15	T_{CL}	7		*5		3.5		ns

Notes: 1. All switching characteristics apply to all valid combinations of process, temperature and supply with a nominal chip power dissipation of 250 mW.

* These parameters are for clock pulses generated within a CLB. For an externally generated pulse, derate these parameters by 20%.

IOB Switching Guidelines



X5433

Speed Grade				-70		-100		-130		Units
	Description	Symbol		Min	Max	Min	Max	Min	Max	
Pad (package pin)	To input (direct)	1	T_{PID}		6		4		3.5	ns
I/O Clock	To input (storage)	5	T_{LI}		11		8		7.5	ns
	To pad-input setup	2	T_{PL}	6		4		2		ns
	To pad-input hold	3	T_{LP}	0		0		4		ns
	Pulse width	4	T_{LW}	7		*5		3.5		ns
	Frequency			70		*100				MHz
Output	To pad (output enabled)	8	T_{OP}		9		7		5.5	ns
Three-state	To pad begin hi-Z	9	T_{THZ}		15		11		7	ns
	To pad end hi-Z	10	T_{TON}		15		13		11	ns
<u>RESET</u>	To input (storage)	6	T_{RI}		25		17		15	ns
	To input clock	7	T_{RC}	20		14		10		ns

Note: Timing is measured at 0.5 V_{CC} levels with 50 pF output load.

*These parameters are for clock pulses generated within an LCA device. For an externally applied clock, derate these parameters by 20%.