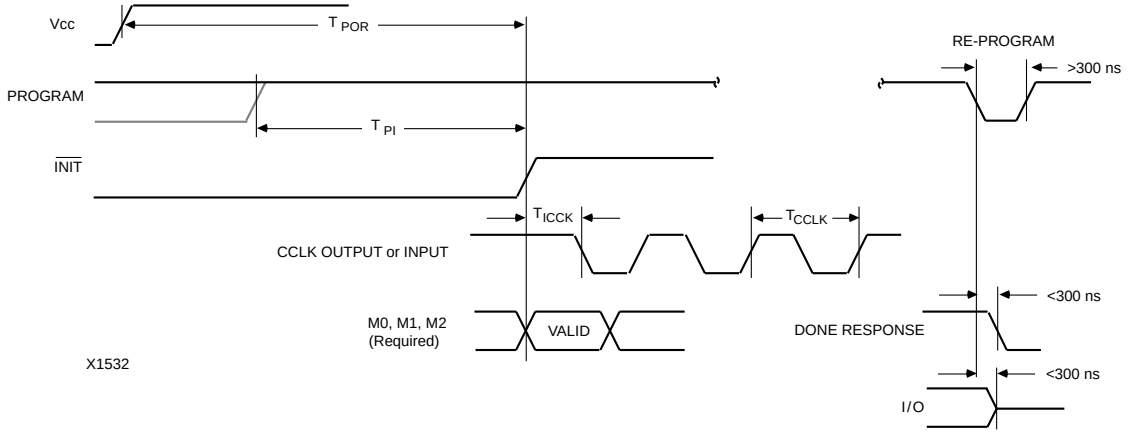
Configuration Switching Characteristics



Master Modes

Description		Symbol	Min	Max	Units
Power-On Reset	M0 = High	T_{POR}	10	40	ms
	M0 = Low	T_{POR}	40	130	ms
Program Latency		T_{PI}	30	200	µs per CLB column
CCLK (output) Delay		T_{ICCK}	40	250	µs
CCLK (output) Period, slow		T_{CCLK}	640	2000	ns
CCLK (output) Period, fast		T_{CCLK}	80	250	ns

Slave and Peripheral Modes

Description	Symbol	Min	Max	Units
Power-On Reset	T_{POR}	10	33	ms
Program Latency	T_{PI}	30	200	µs per CLB column
CCLK (input) Delay (required)	T_{ICCK}	4		µs
CCLK (input) Period (required)	T_{CCLK}	100		ns

XC4000E Switching Characteristics

Definition of Terms

In the following tables, some specifications may be designated as Advanced or Preliminary. These terms are defined as follows:

Advanced: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or device families. Use as estimates, not for production.

Preliminary: Based on preliminary characterization of thirty devices. Numbers are subject to change after further characterization, but are considered fairly stable.

Unmarked: Specifications not identified as either Advanced or Preliminary are final. Further changes are unusual but occasionally occur. All specifications are subject to change without notice.

XC4000E Operating Conditions

Symbol	Description		Min	Max	Units
V_{CC}	Supply voltage relative to GND, T_J = -0 °C to +85°C	Commercial	4.75	5.25	V
	Supply voltage relative to GND, T_J = -40°C to +100°C	Industrial	4.5	5.5	V
	Supply voltage relative to GND, T_C = -55°C to +125°C	Military	4.5	5.5	V
V_{IH}	High-level input voltage	TTL inputs	2.0	V_{CC}	V
		CMOS inputs	70%	100%	V_{CC}
V_{IL}	Low-level input voltage	TTL inputs	0	0.8	V
		CMOS inputs	0	20%	V_{CC}
T_{IN}	Input signal transition time (Note 2)			250	ns

Note 1: At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.
Note 2: Typical value only. Not tested or characterized.

XC4000E DC Characteristics Over Operating Conditions

Symbol	Description		Min	Max	Units
V_{OH}	High-level output voltage @ I_{OH} = -4.0mA, V_{CC} min	TTL outputs	2.4		V
	High-level output voltage @ I_{OH} = -1.0mA, V_{CC} min	CMOS outputs	V_{CC}-0.5		V
V_{OL}	Low-level output voltage @ I_{OL} = 12.0mA, V_{CC} min (Note 1)	TTL outputs		0.4	V
		CMOS outputs		0.4	V
I_{CCO}	Quiescent FPGA supply current (Note 2)	TTL input levels		10	mA
		CMOS input levels		1	mA
I_L	Input or output leakage current		-10	+10	µA
C_{IN}	Input capacitance (sample tested)	PQFP and MQFP packages		10	pF
		Other packages		16	pF
I_{RIN}	Pad pull-up (when selected) @ V_{IN} = 0V (sample tested)		0.02	0.25	mA
I_{RLL}	Horizontal Longline pull-up (when selected) @ logic Low		0.2	2.5	mA

Note 1: With 50% of the outputs simultaneously sinking 12mA, up to a maximum of 64 pins.
Note 2: With no output current loads, no active input or Longline pull-up resistors, all package pins at Vcc or GND, and the FPGA configured with a MakeBits Tie option.

XC4000E Absolute Maximum Ratings

Symbol	Description			Units
V_{CC}	Supply voltage relative to GND		-0.5 to +7.0	V
V_{IN}	Input voltage relative to GND (Note 1)		-0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output (Note 1)		-0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)		-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)		+260	°C
T_J	Junction temperature	Ceramic packages	+150	°C
		Plastic packages	+125	°C

Note 1: Maximum DC overshoot or undershoot above Vcc or below GND must be limited to either 0.5 V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to -2.0 V or overshoot to Vcc + 2.0 V, provided this over- or undershoot lasts less than 20 ns.

Note 2: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

XC4000E Global Buffer Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions.

		Speed Grade	-4	-3	-2		Units
Description	**Symbol**	**Device**	**Max**	**Max**	**Max**		
From pad through Primary buffer, to any clock K	T_{PG}	XC4003E		4.7	4.0		ns
		XC4005E		4.7	4.0		ns
		XC4006E		5.3	4.5		ns
		XC4008E		6.1	5.2		ns
		XC4010E		6.3	5.4		ns
		XC4013E		6.8	5.8		ns
		XC4020E		7.0	6.2		ns
		XC4025E		7.2	6.3		ns
From pad through Secondary buffer, to any clock K	T_{SG}	XC4003E		5.2	4.4		ns
		XC4005E		5.2	4.4		ns
		XC4006E		5.8	4.9		ns
		XC4008E		6.6	5.6		ns
		XC4010E		6.8	5.8		ns
		XC4013E		7.3	6.2		ns
		XC4020E		7.5	6.6		ns
		XC4025E		7.7	6.8		ns
			PRELIMINARY		**ADVANCED**		

XC4000E Wide Decoder Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions.

		Speed Grade	-4	-3	-2		Units
Description	**Symbol**	**Device**	**Max**	**Max**	**Max**		
Full length, both pull-ups, inputs from IOB I-pins	T_{WAF}	XC4003E		5.0	4.3		ns
		XC4005E		6.0	5.1		ns
		XC4006E		7.0	6.2		ns
		XC4008E		8.0	7.0		ns
		XC4010E		9.0	8.1		ns
		XC4013E		11.0	9.9		ns
		XC4020E		13.9	12.5		ns
		XC4025E		16.9	15.2		ns
Full length, both pull-ups, inputs from internal logic	T_{WAFL}	XC4003E		7.0	6.0		ns
		XC4005E		8.0	6.8		ns
		XC4006E		9.0	7.9		ns
		XC4008E		10.0	8.8		ns
		XC4010E		11.0	9.7		ns
		XC4013E		13.0	11.7		ns
		XC4020E		15.5	14.0		ns
		XC4025E		18.9	17.0		ns
Half length, one pull-up, inputs from IOB I-pins	T_{WAO}	XC4003E		6.0	5.1		ns
		XC4005E		7.0	6.0		ns
		XC4006E		8.0	6.8		ns
		XC4008E		9.0	7.9		ns
		XC4010E		10.0	8.8		ns
		XC4013E		12.0	10.8		ns
		XC4020E		15.0	13.5		ns
		XC4025E		17.6	15.8		ns
Half length, one pull-up, inputs from internal logic	T_{WAOL}	XC4003E		8.0	6.8		ns
		XC4005E		9.0	7.7		ns
		XC4006E		10.0	8.5		ns
		XC4008E		11.0	9.4		ns
		XC4010E		12.0	10.2		ns
		XC4013E		14.0	11.9		ns
		XC4020E		16.8	14.3		ns
		XC4025E		19.6	16.7		ns
				PRELIMINARY	**ADVANCED**		

Note 1: These values include a minimum load. The values reported by LCA2XNF -S include only a portion of this delay, therefore the values cannot be directly compared. Use XDelay to determine the delay for each destination.

Note 2: These delays are specified from the decoder input to the decoder output. For pin-to-pin delays, add the input delay (T_{PID}) and output delay (T_{OPF} or T_{OPS}), as listed under "IOB Switching Characteristic Guidelines."

XC4000E Horizontal Longline Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions.

		Speed Grade	-4	-3	-2		Units
Description	**Symbol**	**Device**	**Max**	**Max**	**Max**		
TBUF driving a Horizontal Longline (LL):	T_{IO1}	XC4003E		4.2	3.4		ns
		XC4005E		5.0	4.0		ns
I going High or Low to LL going High or Low, while T is Low.		XC4006E		5.9	4.7		ns
		XC4008E		6.3	5.0		ns
Buffer is constantly active.		XC4010E		6.4	5.1		ns
		XC4013E		7.2	5.7		ns
(Note1)		XC4020E		8.2	6.6		ns
		XC4025E		9.1	7.3		ns
I going Low to LL going from resistive pull-up High to active Low.	T_{IO2}	XC4003E		4.2	3.6		ns
		XC4005E		5.3	4.5		ns
TBUF configured as open-drain.		XC4006E		6.4	5.4		ns
		XC4008E		6.8	5.8		ns
(Note1)		XC4010E		6.9	5.9		ns
		XC4013E		7.7	6.5		ns
		XC4020E		8.7	7.4		ns
		XC4025E		9.6	8.2		ns
T going Low to LL going from resistive pull-up or floating High to active Low.	T_{ON}	XC4003E		4.6	3.9		ns
		XC4005E		6.0	5.4		ns
TBUF configured as open-drain or active buffer with I = Low.		XC4006E		6.7	5.7		ns
		XC4008E		7.1	6.0		ns
(Note1)		XC4010E		7.3	6.2		ns
		XC4013E		7.5	6.4		ns
		XC4020E		8.4	7.1		ns
		XC4025E		8.4	7.1		ns
T going High to TBUF going inactive, not driving LL	T_{OFF}	All devices		1.5	1.3		ns
T going High to LL going from Low to High, pulled up by a single resistor.	T_{PUS}	XC4003E		14.0	11.9		ns
		XC4005E		16.0	13.6		ns
(Note 2)		XC4006E		18.0	15.3		ns
		XC4008E		20.0	17.0		ns
		XC4010E		22.0	18.7		ns
		XC4013E		26.0	22.1		ns
		XC4020E		32.5	27.6		ns
		XC4025E		39.1	33.2		ns
T going High to LL going from Low to High, pulled up by two resistors.	T_{PUF}	XC4003E		7.0	6.0		ns
		XC4005E		8.0	6.8		ns
(Note1)		XC4006E		9.0	7.7		ns
		XC4008E		10.0	8.5		ns
		XC4010E		11.0	9.4		ns
		XC4013E		13.0	11.0		ns
		XC4020E		14.8	12.6		ns
		XC4025E		16.5	14.0		ns
			PRELIMINARY		**ADVANCED**		

Note 1: These values include a minimum load. The values reported by LCA2XNF -S include only a portion of this delay, therefore the values cannot be directly compared. Use XDelay to determine the delay for each destination.

Note 2: This value includes a minimum load. The value reported by LCA2XNF -S is increased to allow for potentially heavy loading, therefore the values cannot be directly compared. Use XDelay to determine the delay for each destination.

XC4000E CLB Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000E devices unless otherwise noted.

Speed Grade		**-4**		**-3**		**-2**			
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**		
Combinatorial Delays									
F/G inputs to X/Y outputs	T_{ILO}				2.0		1.6		
F/G inputs via H' to X/Y outputs	T_{IHO}				4.3		2.7		
C inputs via SR through H' to X/Y outputs	T_{HH0O}				3.3		2.4		
C inputs via H' to X/Y outputs	T_{HH1O}				3.6		2.2		
C inputs via DIN through H' to X/Y outputs	T_{HH2O}				3.6		2.6		
CLB Fast Carry Logic									
Operand inputs (F1, F2, G1, G4) to COUT	T_{OPCY}				2.6		2.1		
Add/Subtract input (F3) to COUT	T_{ASCY}				4.4		3.7		
Initialization inputs (F1, F3) to COUT	T_{INCY}				1.7		1.4		
CIN through function generators to X/Y outputs	T_{SUM}				3.3		2.6		
CIN to COUT, bypass function generators	T_{BYP}				0.7		0.6		
Sequential Delays									
Clock K to outputs Q	T_{CKO}				2.8		2.8		
Setup Time before Clock K									
F/G inputs	T_{ICK}			3.0		2.4			
F/G inputs via H'	T_{IHCK}			4.6		3.9			
C inputs via H0 through H'	T_{HH0CK}			3.6		3.5			
C inputs via H1 through H'	T_{HH1CK}			4.1		3.3			
C inputs via H2 through H'	T_{HH2CK}			3.8		3.7			
C inputs via DIN	T_{DICK}			2.4		2.0			
C inputs via EC	T_{ECCK}			3.0		2.6			
C inputs via S/R, going Low (inactive)	T_{RCK}			4.0		4.0			
C_{IN} input via F'/G'	T_{CCK}								
C_{IN} input via F'/G' and H'	T_{CHCK}								
		PRELIMINARY				**ADVANCED**			

XC4000E CLB Switching Characteristic Guidelines (continued)

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000E devices unless otherwise noted.

Speed Grade		**-4**		**-3**		**-2**			
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**		
Hold Time after Clock K									
F/G inputs	T_{CKI}			0		0			
F/G inputs via H'	T_{CKIH}			0		0			
C inputs via H0 through H'	T_{CKHH0}			0		0			
C inputs via H1 through H'	T_{CKHH1}			0		0			
C inputs via H2 through H'	T_{CKHH2}			0		0			
C inputs via DIN	T_{CKDI}			0		0			
C inputs via EC	T_{CKEC}			0		0			
C inputs via SR, going Low (inactive)	T_{CKR}			0		0			
Clock									
Clock High time	T_{CH}			4.0		4.0			
Clock Low time	T_{CL}			4.0		4.0			
Set/Reset Direct									
Width (High)	T_{RPW}			4.0		4.0			
Delay from C inputs via S/R, going High to Q	T_{RIO}				4.0		4.0		
Master Set/Reset (Note 1)									
Width (High or Low)	T_{MRW}			11.5		11.5			
Delay from Global Set/Reset net to Q	T_{MRQ}				18.7		17.4		
Toggle Frequency (MHz)	F_{TOG}				142				
		PRELIMINARY				**ADVANCED**			

Note 1: Timing is based on the XC4005E. For other devices see the XACT timing calculator.

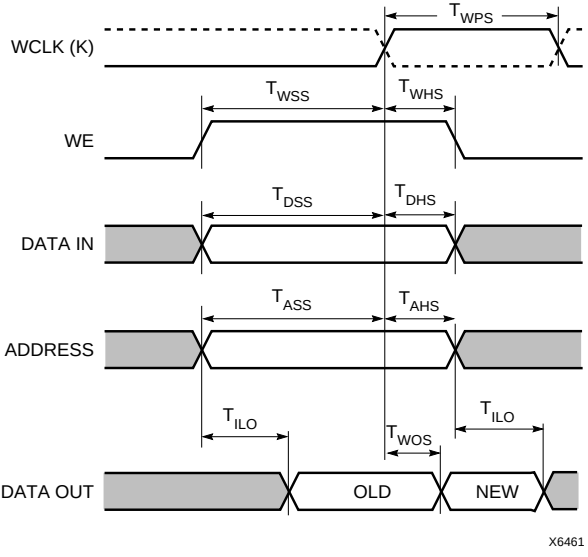
XC4000E CLB Edge-Triggered (Synchronous) RAM Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000E devices unless otherwise noted.

Speed Grade			-4		-3		-2			
Description	**Size**	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**		
Write Operation										
Address write cycle time	16x2	T_{WCS}			14.4		11.6			
(clock K period)	32x1	T_{WCTS}			14.4		11.6			
Clock K pulse width	16x2	T_{WPS}			7.2	1 ms	5.8	1 ms		
(active edge)	32x1	T_{WPTS}			7.2	1 ms	5.8	1 ms		
Address setup time	16x2	T_{ASS}			2.4		2.0			
before clock K	32x1	T_{ASTS}			2.4		2.0			
Address hold time	16x2	T_{AHS}			0		0			
after clock K	32x1	T_{AHTS}			0		0			
DIN setup time	16x2	T_{DSS}			3.2		2.7			
before clock K	32x1	T_{DSTS}			1.9		1.7			
DIN hold time	16x2	T_{DHS}			0		0			
after clock K	32x1	T_{DHTS}			0		0			
WE setup time	16x2	T_{WSS}			2.0		1.6			
before clock K	32x1	T_{WSTS}			2.0		1.6			
WE hold time	16x2	T_{WHS}			0		0			
after clock K	32x1	T_{WHTS}			0		0			
Data valid	16x2	T_{WOS}				8.8		6.3		
after clock K	32x1	T_{WOTS}				10.3		7.4		
			PRELIMINARY				**ADVANCED**			

Note 1: Timing for the 16x1 RAM option is identical to 16x2 RAM timing.
Note 2: Applicable Read timing specifications are identical to Level-Sensitive Read timing.



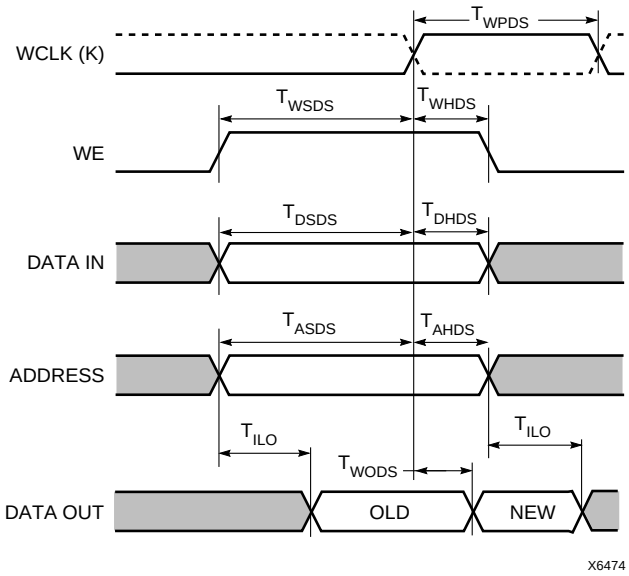
XC4000E CLB Edge-Triggered (Synchronous) Dual-Port RAM Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000E devices unless otherwise noted.

	Speed Grade		-4		-3		-2			
Description	**Size**	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**		
Write Operation										
Address write cycle time (clock K period)	16x1	T_{WCDS}			14.4		11.6			
Clock K pulse width (active edge)	16x1	T_{WPDS}			7.2	1 ms	5.8	1 ms		
Address setup time before clock K	16x1	T_{ASDS}			2.5		2.1			
Address hold time after clock K	16x1	T_{AHDS}			0		0			
DIN setup time before clock K	16x1	T_{DSDS}			1.9		1.6			
DIN hold time after clock K	16x1	T_{DHDS}			0		0			
WE setup time before clock K	16x1	T_{WSDS}			2.0		1.6			
WE hold time after clock K	16x1	T_{WHDS}			0		0			
Data valid after clock K	16x1	T_{WODS}				7.8		6.2		
			PRELIMINARY				**ADVANCED**			

Note: Applicable Read timing specifications are identical to16x2 Level-Sensitive Read timing.



XC4000E CLB Level-Sensitive RAM Switching Characteristic Guidelines

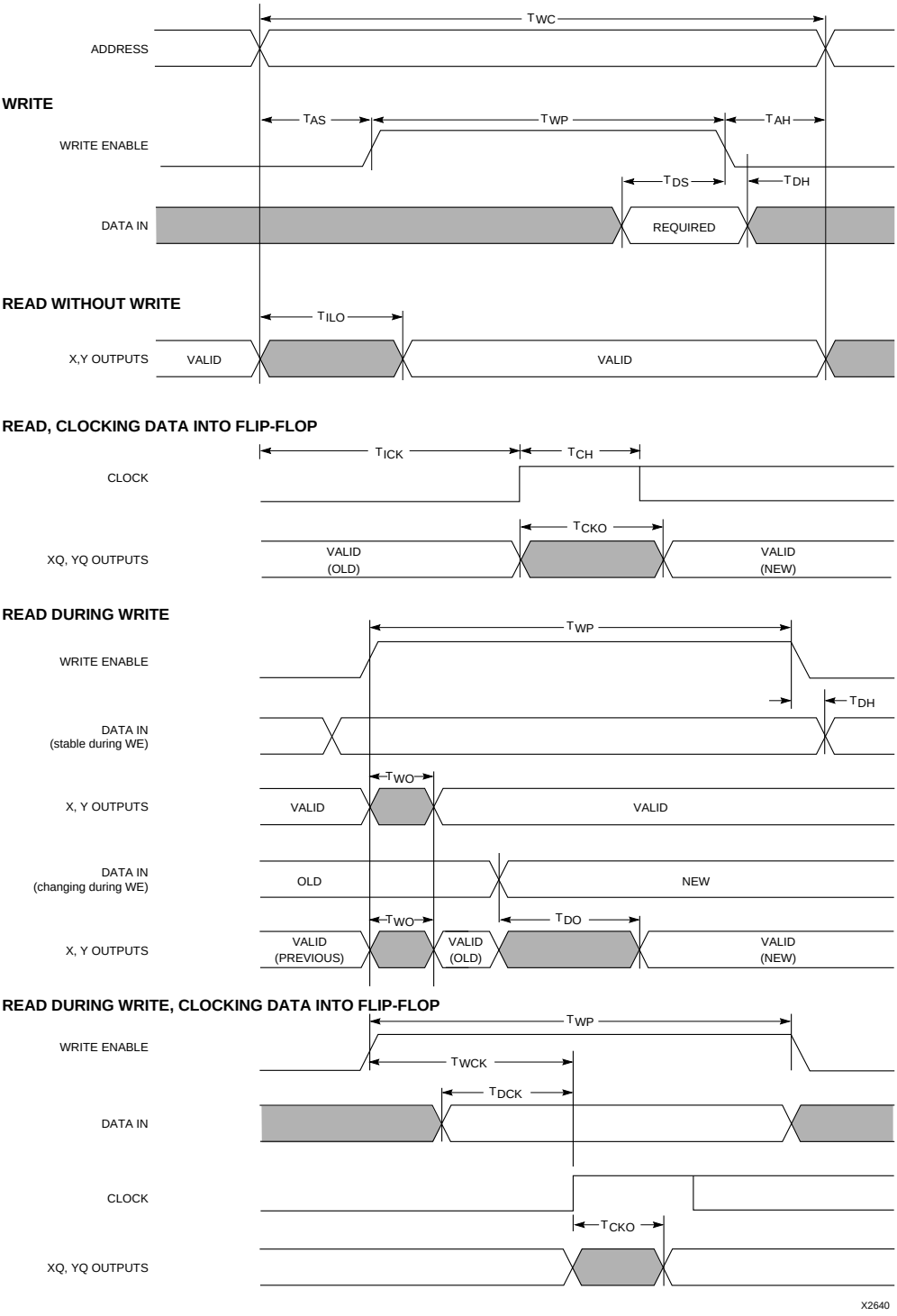
Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000E devices unless otherwise noted.

Speed Grade			-4		-3		-2			
Description	**Size**	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**		
Write Operation										
Address write cycle time	16x2	T_{WC}			8.0		8.0			
	32x1	T_{WCT}			8.0		8.0			
Write Enable pulse width	16x2	T_{WP}			4.0		4.0			
(High)	32x1	T_{WPT}			4.0		4.0			
Address setup time	16x2	T_{AS}			2.0		2.0			
before WE	32x1	T_{AST}			2.0		2.0			
Address hold time	16x2	T_{AH}			2.0		2.0			
after end of WE	32x1	T_{AHT}			2.0		2.0			
DIN setup time	16x2	T_{DS}			2.2		0.8			
before end of WE	32x1	T_{DST}			2.2		0.8			
DIN hold time	16x2	T_{DH}			2.0		2.0			
after end of WE	32x1	T_{DHT}			2.0		2.0			
Read Operation										
Address read cycle time	16x2	T_{RC}			3.1		2.6			
	32x1	T_{RCT}			5.5		3.8			
Data valid after address	16x2	T_{ILO}				2.0		1.6		
change (no Write Enable)	32x1	T_{IHO}				4.3		2.7		
Read Operation, Clocking Data into Flip-Flop										
Address setup time	16x2	T_{ICK}			3.0		2.4			
before clock K	32x1	T_{IHCK}			4.6		3.9			
Read During Write										
Data valid after WE goes	16x2	T_{WO}				6.0		4.9		
active (DIN stable	32x1	T_{WOT}				7.3		5.6		
before WE)										
Data valid after DIN	16x2	T_{DO}				6.6		5.8		
(DIN changes during WE)	32x1	T_{DOT}				7.6		6.2		
Read During Write, Clocking Data into Flip-Flop										
WE setup time	16x2	T_{WCK}			6.0		5.1			
before clock K	32x1	T_{WCKT}			6.8		5.8			
Data setup time	16x2	T_{DCK}			5.2		4.4			
before clock K	32x1	T_{DCKT}			6.2		5.3			
			PRELIMINARY				**ADVANCED**			

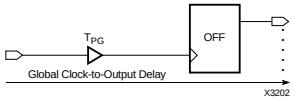
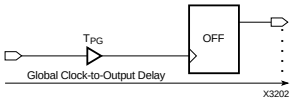
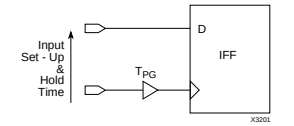
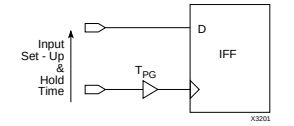
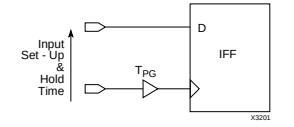
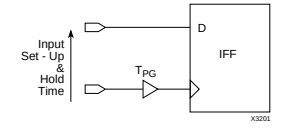
Note: Timing for the 16x1 RAM option is identical to 16x2 RAM timing.

XC4000E CLB Level-Sensitive RAM Timing Characteristics



XC4000E Guaranteed Input and Output Parameters (Pin-to-Pin, TTL Inputs)

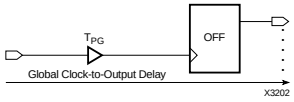
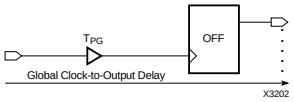
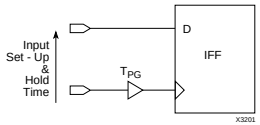
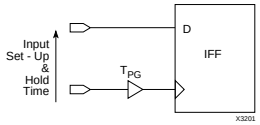
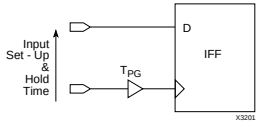
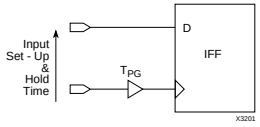
All values listed below are tested directly, and guaranteed over the operating conditions. The same parameters can also be derived indirectly from the IOB and Global Buffer specifications. The XACT delay calculator uses this indirect method. When there is a discrepancy between the two methods, the values listed below should be used, and the derived values must be ignored. All values are expressed in units of nanoseconds.

Description	Symbol	Device	Speed Grade -4	-3	-2
Global Clock to Output (fast) using OFF 	T_{ICKOF} (Max)	XC4003E XC4005E XC4006E XC4008E XC4010E XC4013E XC4020E XC4025E		10.2 10.7 10.7 10.8 10.9 11.0 11.0 12.6	8.7 9.1 9.1 9.2 9.3 9.4 9.4 10.7
Global Clock to Output (slew-limited) using OFF 	T_{ICKO} (Max)	XC4003E XC4005E XC4006E XC4008E XC4010E XC4013E XC4020E XC4025E		14.0 14.7 14.7 14.8 14.9 15.0 15.1 15.3	11.5 12.0 12.0 12.1 12.2 12.8 12.8 13.0
Input Setup Time, using IFF (no delay) 	T_{PSUF} (Min)	XC4003E XC4005E XC4006E XC4008E XC4010E XC4013E XC4020E XC4025E		2.3 1.2 1.0 0.6 0.2 0 0 0	2.3 1.2 1.0 0.6 0.2 0 0 0
Input Hold Time, using IFF (no delay) 	T_{PHF} (Min)	XC4003E XC4005E XC4006E XC4008E XC4010E XC4013E XC4020E XC4025E		4.0 4.5 4.7 5.1 5.5 6.5 6.7 7.0	4.0 4.5 4.7 5.1 5.5 5.5 5.7 5.9
Input Setup Time, using IFF (with delay) 	T_{PSU} (Min)	XC4003E XC4005E XC4006E XC4008E XC4010E XC4013E XC4020E XC4025E		7.0 7.0 7.0 7.0 7.0 7.0 7.0 7.6	6.0 6.0 6.0 6.0 6.0 6.0 6.0 6.5
Input Hold Time, using IFF (with delay) 	T_{PH} (Min)	XC4003E XC4005E XC4006E XC4008E XC4010E XC4013E XC4020E XC4025E		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0

OFF = Output Flip-Flop IFF = Input Flip-Flop or Latch **PRELIMINARY** **ADVANCED**

XC4000E Guaranteed Input and Output Parameters (Pin-to-Pin, CMOS Inputs)

All values listed below are tested directly, and guaranteed over the operating conditions. The same parameters can also be derived indirectly from the IOB and Global Buffer specifications. The XACT delay calculator uses this indirect method. When there is a discrepancy between the two methods, the values listed below should be used, and the derived values must be ignored. All values are expressed in units of nanoseconds.

	Speed Grade		-4	-3	-2	
Description	**Symbol**	**Device**				
Global Clock to Output (fast) using OFF 	T_{CICKOF} (Max)	XC4003E XC4005E XC4006E XC4008E XC4010E XC4013E XC4020E XC4025E				
Global Clock to Output (slew-limited) using OFF 	T_{CICKO} (Max)	XC4003E XC4005E XC4006E XC4008E XC4010E XC4013E XC4020E XC4025E				
Input Setup Time, using IFF (no delay) 	T_{CPSUF} (Min)	XC4003E XC4005E XC4006E XC4008E XC4010E XC4013E XC4020E XC4025E				
Input Hold Time, using IFF (no delay) 	T_{CPHF} (Min)	XC4003E XC4005E XC4006E XC4008E XC4010E XC4013E XC4020E XC4025E				
Input Setup Time, using IFF (with delay) 	T_{CPSU} (Min)	XC4003E XC4005E XC4006E XC4008E XC4010E XC4013E XC4020E XC4025E				
Input Hold Time, using IFF (with delay) 	T_{CPH} (Min)	XC4003E XC4005E XC4006E XC4008E XC4010E XC4013E XC4020E XC4025E		0 0 0 0 0 0 0 0	0 0 0 0 0 0 0 0	
OFF = Output Flip-Flop	IFF = Input Flip-Flop or Latch		**PRELIMINARY**		**ADVANCED**	

XC4000E IOB Input Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000E devices unless otherwise noted.

Speed Grade			-4		-3		-2			
Description	**Symbol**	**Device**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**		
Propagation Delays (TTL Inputs)										
Pad to I1, I2	T_{PID}	All devices				2.5		2.0		
Pad to I1, I2 via transparent latch,										
no delay	T_{PLI}	All devices				3.6		3.6		
with delay	T_{PDLI}	XC4003E				9.3		7.0		
		XC4005E				9.6		7.3		
		XC4006E				10.2		7.8		
		XC4008E				10.6		8.1		
		XC4010E				10.8		8.2		
		XC4013E				11.2		8.5		
		XC4020E				12.4		9.5		
		XC4025E				13.7		9.5		
(CMOS Inputs)										
Pad to I1, I2	T_{PIDC}	All devices				4.1		3.7		
Pad to I1, I2 via transparent latch,										
no delay	T_{PLIC}	All devices				6.8		6.2		
with delay	T_{PDLIC}	XC4003E				12.4		11.0		
		XC4005E				13.2		11.9		
		XC4006E				13.4		12.1		
		XC4008E				13.8		12.4		
		XC4010E				14.0		12.6		
		XC4013E				14.4		13.0		
		XC4020E				15.6		14.0		
		XC4025E				15.6		14.0		
(TTL or CMOS)										
Clock (IK) to I1, I2 (flip-flop)	T_{IKRI}	All devices				2.8		2.8		
Clock (IK) to I1, I2										
(latch enable, active Low)	T_{IKLI}	All devices				4.0		3.9		
Hold Times (Note 1)										
Pad to Clock (IK), no delay	T_{IKPI}	All devices			0		0			
with delay	T_{IKPID}	All devices			0		0			
Clock Enable (EC) to Clock (IK),										
no delay	T_{IKEC}	All devices			1.5		0.9			
with delay	T_{IKECD}	All devices			0		0			
			PRELIMINARY				**ADVANCED**			

Note 1: Input pad setup and hold times are specified with respect to the internal clock (IK). For setup and hold times with respect to the clock input pin, see the pin-to-pin parameters in the Guaranteed Input and Output Parameters table.

Note 2: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

XC4000E IOB Input Switching Characteristic Guidelines (continued)

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000E devices unless otherwise noted.

Speed Grade			-4		-3		-2			
Description	**Symbol**	**Device**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**		
Setup Times (TTL Inputs)										
Pad to Clock (IK), no delay	T_{PICK}	All devices			2.6		1.7			
with delay	T_{PICKD}	XC4003E			8.2		5.5			
		XC4005E			8.7		5.5			
		XC4006E			9.2		6.6			
		XC4008E			9.6		6.9			
		XC4010E			9.8		7.0			
		XC4013E			10.2		7.3			
		XC4020E			11.4		8.2			
		XC4025E			11.4		8.2			
(CMOS Inputs)										
Pad to Clock (IK), no delay	T_{PICKC}	All devices			3.3		2.4			
with delay	T_{PICKDC}	XC4003E			8.8		6.2			
		XC4005E			9.7		6.2			
		XC4006E			9.9		7.3			
		XC4008E			10.3		7.6			
		XC4010E			10.5		7.7			
		XC4013E			10.9		8.0			
		XC4020E			12.1		8.9			
		XC4025E			12.1		8.9			
(TTL or CMOS)										
Clock Enable (EC) to Clock (IK),										
no delay	T_{ECIK}	All devices			2.5		2.0			
with delay	T_{ECIKD}	XC4003E			8.1		5.6			
		XC4005E			8.5		5.6			
		XC4006E			9.1		6.9			
		XC4008E			9.5		7.2			
		XC4010E			9.7		7.3			
		XC4013E			10.1		7.6			
		XC4020E			11.3		8.5			
		XC4025E			11.3		8.5			
			PRELIMINARY				**ADVANCED**			

Note 1: Input pad setup and hold times are specified with respect to the internal clock (IK). For setup and hold times with respect to the clock input pin, see the pin-to-pin parameters in the Guaranteed Input and Output Parameters table.

Note 2: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

XC4000E IOB Output Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000E devices unless otherwise noted.

Speed Grade		**-4**		**-3**		**-2**			
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**		
Propagation Delays (TTL Output Levels)									
Clock (OK) to Pad, fast	T_{OKPOF}				6.5		4.5		
slew-rate limited	T_{OKPOS}				9.5		7.0		
Output (O) to Pad, fast	T_{OPF}				5.5		4.8		
slew-rate limited	T_{OPS}				8.5		7.3		
3-state to Pad hi-Z (slew-rate independent)	T_{TSHZ}				4.2		3.8		
3-state to Pad active and valid, fast	T_{TSONF}				8.1		7.3		
slew-rate limited	T_{TSONS}				11.1		9.8		
Propagation Delays (CMOS Output Levels)									
Clock (OK) to Pad, fast	T_{OKPOFC}				7.8		7.0		
slew-rate limited	T_{OKPOSC}				11.6		10.4		
Output (O) to Pad, fast	T_{OPFC}				9.7		8.7		
slew-rate limited	T_{OPSC}				13.4		12.1		
3-state to Pad hi-Z (slew-rate independent)	T_{TSHZC}				4.3		3.9		
3-state to Pad active and valid, fast	T_{TSONFC}				7.6		6.8		
slew-rate limited	T_{TSONSC}				11.4		10.2		
		PRELIMINARY				**ADVANCED**			

Note 1: Output timing is measured at pin threshold, with 50pF external capacitive loads (incl. test fixture). Slew-rate limited output rise/fall times are approximately two times longer than fast output rise/fall times. For the effect of capacitive loads on ground bounce, see the “Additional XC4000 Data” section of the Programmable Logic Data Book.

Note 2: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

XC4000E IOB Output Switching Characteristic Guidelines (continued)

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000E devices unless otherwise noted.

Speed Grade		-4		-3		-2			
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**		
Setup and Hold									
Output (O) to clock (OK) setup time	T_{OOK}			4.6		3.8			
Output (O) to clock (OK) hold time	T_{OKO}			0		0			
Clock Enable (EC) to clock (OK) setup	T_{ECOK}			3.5		2.5			
Clock Enable (EC) to clock (OK) hold	T_{OKEC}			1.2		0.5			
Clock									
Clock High	T_{CH}			4.0		4.0			
Clock Low	T_{CL}			4.0		4.0			
Global Set/Reset (Note 3)									
Delay from GSR net through Q to I1, I2	T_{RRI}				7.8		6.8		
Delay from GSR net to Pad	T_{RPO}				11.8		8.7		
GSR width	T_{MRW}			11.5		11.5			
		PRELIMINARY				**ADVANCED**			

Note 1: Output timing is measured at pin threshold, with 50pF external capacitive loads (incl. test fixture). Slew-rate limited output rise/fall times are approximately two times longer than fast output rise/fall times. For the effect of capacitive loads on ground bounce, see the “Additional XC4000 Data” section of the Programmable Logic Data Book.

Note 2: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

Note 3: Timing is based on the XC4005E. For other devices see the XACT timing calculator.

XC4000E Boundary Scan (JTAG) Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000E devices unless otherwise noted.

Speed Grade		**-4**		**-3**		**-2**			
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**		
Setup and Hold									
Input (TDI) to clock (TCK) setup time	T_{TDITCK}								
Input (TDI) to clock (TCK) hold time	T_{TCKTDI}								
Input (TMS) to clock (TCK) setup time	T_{TMSTCK}								
Input (TMS) to clock (TCK) hold time	T_{TCKTMS}								
Propagation Delay									
Clock (TCK) to Pad (TDO)	T_{TCKPO}								
Clock									
Clock (TCK) High	T_{TCKH}								
Clock (TCK) Low	T_{TCKL}								
Power-On Reset									
JTAG operation after valid Vcc	T_{RJTAG}								
		PRELIMINARY				**ADVANCED**			

Note 1: Input pad setup and hold times are specified with respect to the internal clock (IK). For setup and hold times with respect to the clock input pin, see the pin-to-pin parameters in the Guaranteed Input and Output Parameters table.

Note 2: Output timing is measured at pin threshold, with 50pF external capacitive loads (incl. test fixture). Slew-rate limited output rise/fall times are approximately two times longer than fast output rise/fall times. For the effect of capacitive loads on ground bounce, see the “Additional XC4000 Data” section of the Programmable Logic Data Book.

Note 3: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

XC4000L Switching Characteristics

Definition of Terms

In the following tables, some specifications may be designated as Advanced or Preliminary. These terms are defined as follows:

Advanced: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or device families. Not to be relied on for designs.

Preliminary: Based on preliminary characterization of thirty devices. Numbers are subject to change after further characterization, but are considered fairly stable.

Unmarked: Specifications not identified as either Advanced or Preliminary are final. Further changes are unusual but occasionally occur. All specifications are subject to change without notice.

XC4000L Operating Conditions

Symbol	Description		Min	Max	Units
V_{CC}	Supply voltage relative to GND, T_J = -0 °C to +85°C	Commercial	3.0	3.6	V
V_{IH}	High-level input voltage		2.0	V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		-0.3	0.8	V
T_{IN}	Input signal transition time (Note 2)			250	ns

Note 1: At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.
Note 2: Typical value only. Not tested or characterized.

XC4000L DC Characteristics Over Operating Conditions

Symbol	Description		Min	Max	Units
V_{OH}	High-level output voltage @ I_{OH} = -4.0mA, V_{CC} min		2.4		V
	High-level output voltage @ I_{OH} = -0.1mA, V_{CC} min		V_{CC}-0.2		V
V_{OL}	Low-level output voltage @ I_{OL} = +4.0mA, V_{CC} min			0.4	V
	Low-level output voltage @ I_{OL} = +0.1mA, V_{CC} min			0.2	V
I_{CCO}	Quiescent FPGA supply current (Note 1)			40	µA
I_L	Input or output leakage current		-20	+20	µA
C_{IN}	Input capacitance (sample tested)	PQFP and MQFP packages		10	pF
		Other packages		16	pF
I_{RIN}	Pad pull-up (when selected) @ V_{IN} = 0V (sample tested)		0.02	0.25	mA
I_{RLL}	Horizontal Longline pull-up (when selected) @ logic Low		0.2	2.5	mA

Note 1: With no output current loads, no active input or Longline pull-up resistors, all package pins at Vcc or GND, and the FPGA configured with a MakeBits Tie option.

XC4000L Absolute Maximum Ratings

Symbol	Description			Units
V_{CC}	Supply voltage relative to GND		-0.5 to +7.0	V
V_{IN}	Input voltage relative to GND (Note 1)		-0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output (Note 1)		-0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)		-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)		+260	°C
T_J	Junction temperature	Ceramic packages	+150	°C
		Plastic packages	+125	°C

Note 1: Maximum DC overshoot or undershoot above Vcc or below GND must be limited to either 0.5 V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to -2.0 V or overshoot to Vcc + 2.0 V, provided this over- or undershoot lasts less than 20 ns.

Note 2: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

XC4000L Global Buffer Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions.

Speed Grade			-6	-5	-4	Units
Description	**Symbol**	**Device**	**Max**	**Max**	**Max**	
From pad through Primary buffer, to any clock K	T_{PG}	XC4005L	8.0	6.0		ns
		XC4010L	9.0	7.0		ns
		XC4013L	10.0	8.0		ns
From pad through Secondary buffer, to any clock K	T_{SG}	XC4005L	9.0	7.0		ns
		XC4010L	10.0	8.0		ns
		XC4013L	11.0	9.0		ns
			ADVANCED			

XC4000L Wide Decoder Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions.

Speed Grade			-6	-5	-4	Units
Description	**Symbol**	**Device**	**Max**	**Max**	**Max**	
Full length, both pull-ups, inputs from IOB I-pins	T_{WAF}	XC4005L XC4010L XC4013L	10.0 13.0 15.0	9.0 12.0 14.0		ns ns ns
Full length, both pull-ups, inputs from internal logic	T_{WAFL}	XC4005L XC4010L XC4013L	13.0 16.0 18.0	12.0 15.0 17.0		ns ns ns
Half length, one pull-up, inputs from IOB I-pins	T_{WAO}	XC4005L XC4010L XC4013L	10.0 13.0 15.0	9.0 12.0 14.0		ns ns ns
Half length, one pull-up, inputs from internal logic	T_{WAOL}	XC4005L XC4010L XC4013L	13.0 16.0 18.0	12.0 15.0 17.0		ns ns ns
			ADVANCED			

Note 1: These values include a minimum load. The values reported by LCA2XNF -S include only a portion of this delay, therefore the values cannot be directly compared. Use XDelay to determine the delay for each destination.

Note 2: These delays are specified from the decoder input to the decoder output. For pin-to-pin delays, add the input delay (T_{PID}) and output delay (T_{OPF} or T_{OPS}), as listed under "IOB Switching Characteristic Guidelines."

XC4000L Horizontal Longline Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions.

Speed Grade			**-6**	**-5**	**-4**	**Units**
Description	**Symbol**	**Device**	**Max**	**Max**	**Max**	
TBUF driving a Horizontal Longline (LL): I going High or Low to LL going High or Low, while T is Low. Buffer is constantly active. (Note1)	T_{IO1}	XC4005L XC4010L XC4013L	10.0 11.7 13.0	7.0 8.5 9.5		ns ns ns
I going Low to LL going from resistive pull-up High to active Low. TBUF configured as open-drain. (Note1)	T_{IO2}	XC4005L XC4010L XC4013L	10.5 12.2 13.5	7.5 9.0 10.0		ns ns ns
T going Low to LL going from resistive pull-up or floating High to active Low. TBUF configured as open-drain or active buffer with I = Low. (Note1)	T_{ON}	XC4005L XC4010L XC4013L	12.0 13.8 15.1	10.0 11.5 12.6		ns ns ns
T going High to TBUF going inactive, not driving LL	T_{OFF}	All devices	3.0	2.0		ns
T going High to LL going from Low to High, pulled up by a single resistor. (Note 2)	T_{PUS}	XC4005L XC4010L XC4013L	26.0 32.0 36.0	22.0 28.0 32.0		ns ns ns
T going High to LL going from Low to High, pulled up by two resistors. (Note1)	T_{PUF}	XC4005L XC4010L XC4013L	12.0 15.0 17.0	10.0 13.0 15.0		ns ns ns
			ADVANCED			

Note 1: These values include a minimum load. The values reported by LCA2XNF -S include only a portion of this delay, therefore the values cannot be directly compared. Use XDelay to determine the delay for each destination.

Note 2: This value includes a minimum load. The value reported by LCA2XNF -S is increased to allow for potentially heavy loading, therefore the values cannot be directly compared. Use XDelay to determine the delay for each destination.

XC4000L CLB Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000L devices unless otherwise noted.

Speed Grade		-6		-5		-4	
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
Combinatorial Delays							
F/G inputs to X/Y outputs	T_{ILO}		6.0		4.5		
F/G inputs via H' to X/Y outputs	T_{IHO}		8.0		7.0		
C inputs via SR through H' to X/Y outputs	T_{HH0O}						
C inputs via H' to X/Y outputs	T_{HH1O}		7.0		5.0		
C inputs via DIN through H' to X/Y outputs	T_{HH2O}						
CLB Fast Carry Logic							
Operand inputs (F1, F2, G1, G4) to COUT	T_{OPCY}		7.0		5.5		
Add/Subtract input (F3) to COUT	T_{ASCY}		8.0		6.0		
Initialization inputs (F1, F3) to COUT	T_{INCY}		6.0		4.0		
CIN through function generators to X/Y outputs	T_{SUM}		8.0		6.0		
CIN to COUT, bypass function generators	T_{BYP}		2.0		1.5		
Sequential Delays							
Clock K to outputs Q	T_{CKO}		5.0		3.0		
Setup Time before Clock K							
F/G inputs	T_{ICK}	6.0		4.5			
F/G inputs via H'	T_{IHCK}	8.0		6.0			
C inputs via H0 through H'	T_{HH0CK}						
C inputs via H1 through H'	T_{HH1CK}	7.0		5.0			
C inputs via H2 through H'	T_{HH2CK}						
C inputs via DIN	T_{DICK}	4.0		3.0			
C inputs via EC	T_{ECCK}	7.0		4.0			
C inputs via S/R, going Low (inactive)	T_{RCK}	6.0		4.5			
C_{IN} input via F'/G'	T_{CCK}						
C_{IN} input via F'/G' and H'	T_{CHCK}						
		ADVANCED					

XC4000L CLB Switching Characteristic Guidelines (continued)

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000L devices unless otherwise noted.

Speed Grade		**-6**		**-5**		**-4**	
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
Hold Time after Clock K							
F/G inputs	T_{CKI}	0		0			
F/G inputs via H'	T_{CKIH}	0		0			
C inputs via H0 through H'	T_{CKHH0}	0		0			
C inputs via H1 through H'	T_{CKHH1}	0		0			
C inputs via H2 through H'	T_{CKHH2}	0		0			
C inputs via DIN	T_{CKDI}	0		0			
C inputs via EC	T_{CKEC}	0		0			
C inputs via SR, going Low (inactive)	T_{CKR}	0		0			
Clock							
Clock High time	T_{CH}	5.0		4.5			
Clock Low time	T_{CL}	5.0		4.5			
Set/Reset Direct							
Width (High)	T_{RPW}	5.0		4.0			
Delay from C inputs via S/R, going High to Q	T_{RIO}		9.0		8.0		
Master Set/Reset (Note 1)							
Width (High or Low)	T_{MRW}	21.0		18.0			
Delay from Global Set/Reset net to Q	T_{MRQ}		33.0		31.0		
Toggle Frequency (MHz)	F_{TOG}						
		ADVANCED					

Note 1: Timing is based on the XC4005L. For other devices see the XACT timing calculator.

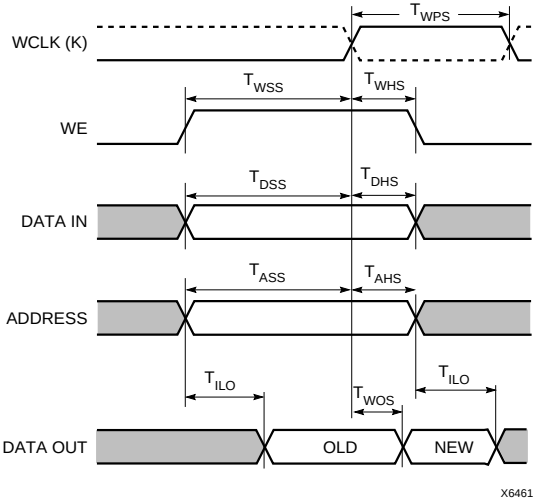
XC4000L CLB Edge-Triggered (Synchronous) RAM Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000L devices unless otherwise noted.

Speed Grade			-6		-5		-4	
Description	**Size**	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
Write Operation								
Address write cycle time	16x2	T_{WCS}						
(clock K period)	32x1	T_{WCTS}						
Clock K pulse width	16x2	T_{WPS}						
(active edge)	32x1	T_{WPTS}						
Address setup time	16x2	T_{ASS}						
before clock K	32x1	T_{ASTS}						
Address hold time	16x2	T_{AHS}						
after clock K	32x1	T_{AHTS}						
DIN setup time	16x2	T_{DSS}						
before clock K	32x1	T_{DSTS}						
DIN hold time	16x2	T_{DHS}						
after clock K	32x1	T_{DHTS}						
WE setup time	16x2	T_{WSS}						
before clock K	32x1	T_{WSTS}						
WE hold time	16x2	T_{WHS}						
after clock K	32x1	T_{WHTS}						
Data valid	16x2	T_{WOS}						
after clock K	32x1	T_{WOTS}						
			ADVANCED					

Note 1. Timing for the 16x1 RAM option is identical to 16x2 RAM timing.
Note 2. Applicable Read timing specifications are identical to Level-Sensitive Read timing.



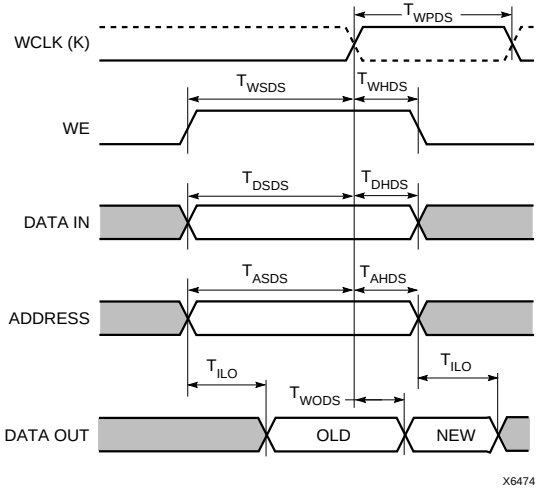
XC4000L CLB Edge-Triggered (Synchronous) Dual-Port RAM Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000L devices unless otherwise noted.

Speed Grade			-6		-5		-4	
Description	**Size**	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
Write Operation								
Address write cycle time (clock K period)	16x1	T_{WCDS}						
Clock K pulse width (active edge)	16x1	T_{WPDS}						
Address setup time before clock K	16x1	T_{ASDS}						
Address hold time after clock K	16x1	T_{AHDS}						
DIN setup time before clock K	16x1	T_{DSDS}						
DIN hold time after clock K	16x1	T_{DHDS}						
WE setup time before clock K	16x1	T_{WSDS}						
WE hold time after clock K	16x1	T_{WHDS}						
Data valid after clock K	16x1	T_{WODS}						
			ADVANCED					

Note: Applicable Read timing specifications are identical to16x2 Level-Sensitive Read timing.



XC4000L CLB Level-Sensitive RAM Switching Characteristic Guidelines

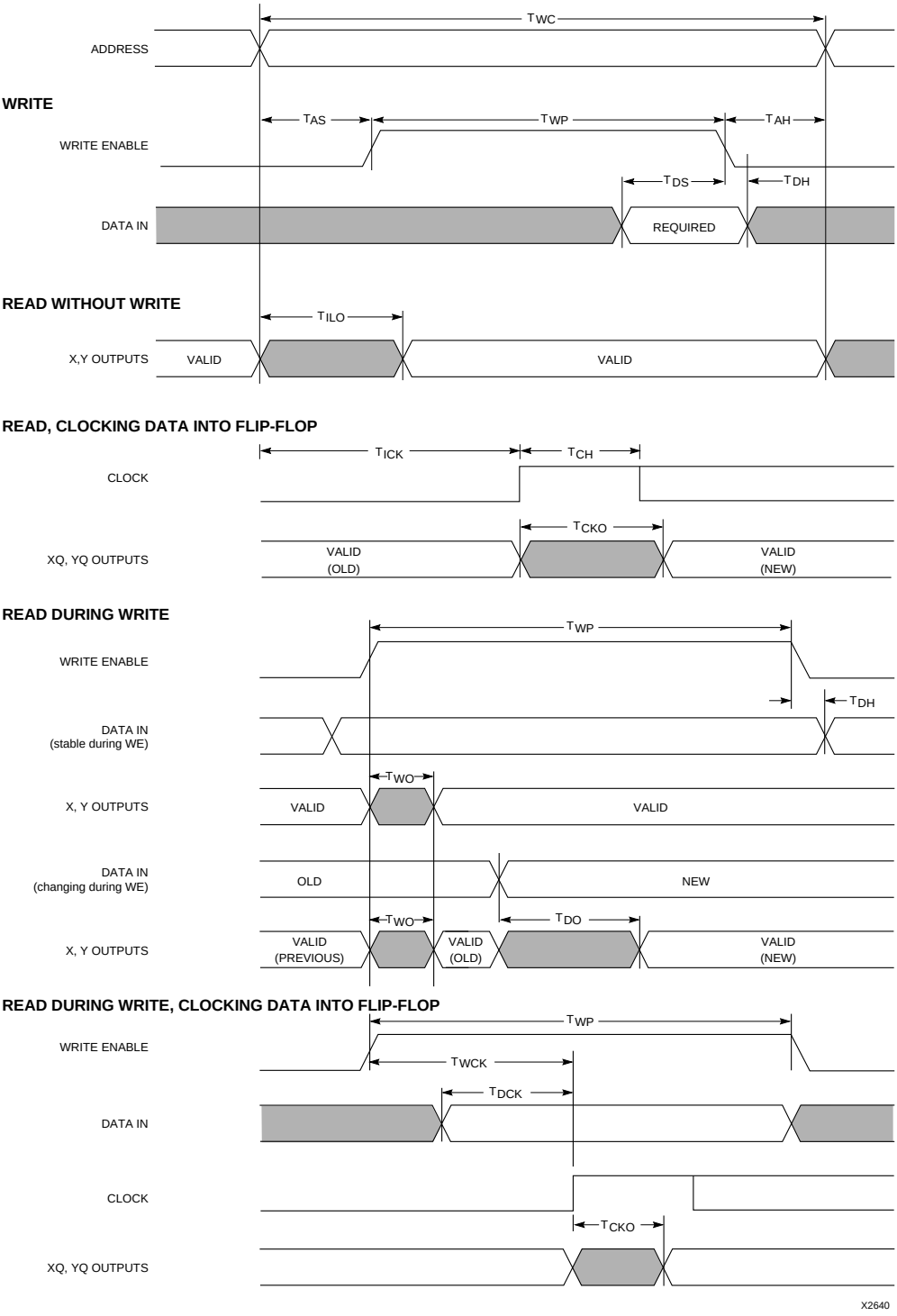
Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000L devices unless otherwise noted.

Speed Grade			-6		-5		-4	
Description	**Size**	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
Write Operation								
Address write cycle time	16x2	T_{WC}	9.0		8.0			
	32x1	T_{WCT}	9.0		8.0			
Write Enable pulse	16x2	T_{WP}	5.0		4.0			
width (High)	32x1	T_{WPT}	5.0		4.0			
Address setup time	16x2	T_{AS}	2.0		2.0			
before WE	32x1	T_{AST}	2.0		2.0			
Address hold time	16x2	T_{AH}	2.0		2.0			
after end of WE	32x1	T_{AHT}	2.0		2.0			
DIN setup time	16x2	T_{DS}	4.0		4.0			
before end of WE	32x1	T_{DST}	5.0		5.0			
DIN hold time	16x2	T_{DH}	2.0		2.0			
after end of WE	32x1	T_{DHT}	2.0		2.0			
Read Operation								
Address read cycle	16x2	T_{RC}	7.0		5.5			
time	32x1	T_{RCT}	10.0		7.5			
Data valid after address	16x2	T_{ILO}		6.0		4.5		
change (no Write Enable)	32x1	T_{IHO}		8.0		7.0		
Read Operation, Clocking Data into Flip-Flop								
Address setup time	16x2	T_{ICK}	6.0		4.5			
before clock K	32x1	T_{IHCK}	8.0		6.0			
Read During Write								
Data valid after WE goes active	16x2	T_{WO}		12.0		10.0		
(DIN stable before WE)	32x1	T_{WOT}		15.0		12.0		
Data valid after DIN	16x2	T_{DO}		11.0		9.0		
(DIN changes during WE)	32x1	T_{DOT}		14.0		11.0		
Read During Write, Clocking Data into Flip-Flop								
WE setup time before clock K	16x2	T_{WCK}	12.0		10.0			
	32x1	T_{WCKT}	15.0		12.0			
Data setup time before clock K	16x2	T_{DCK}	11.0		9.0			
	32x1	T_{DCKT}	14.0		11.0			
			ADVANCED					

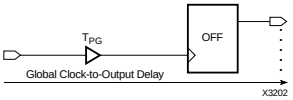
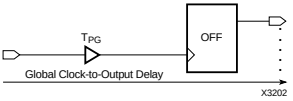
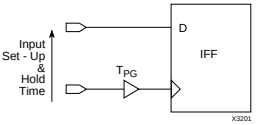
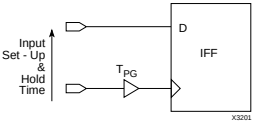
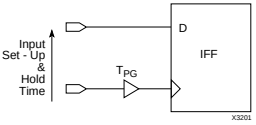
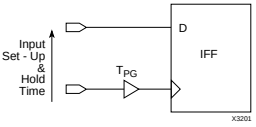
Note: Timing for the 16x1 RAM option is identical to 16x2 RAM timing.

XC4000L CLB Level-Sensitive RAM Timing Characteristics



XC4000L Guaranteed Input and Output Parameters (Pin-to-Pin, CMOS Inputs)

All values listed below are tested directly, and guaranteed over the operating conditions. The same parameters can also be derived indirectly from the IOB and Global Buffer specifications. The XACT delay calculator uses this indirect method. When there is a discrepancy between the two methods, the values listed below should be used, and the derived values must be ignored.

Description	Symbol	Device	-6	-5	-4	Units
Global Clock to Output (fast) using OFF 	T_{ICKOF}	XC4005L XC4010L XC4013L	15.5 16.5 17.5	13.0 14.0 15.0		ns ns ns
	(Max)					
Global Clock to Output (slew-limited) using OFF 	T_{ICKO}	XC4005L XC4010L XC4013L	20.5 21.5 22.5	16.0 17.0 18.0		ns ns ns
	(Max)					
Input Setup Time, using IFF (no delay) 	T_{PSUF}	XC4005L XC4010L XC4013L	2.0 1.0 0.5	1.5 0.5 0		ns ns ns
	(Min)					
Input Hold Time, using IFF (no delay) 	T_{PHF}	XC4005L XC4010L XC4013L	5.5 6.5 7.5	4.5 5.5 6.5		ns ns ns
	(Min)					
Input Setup Time, using IFF (with delay) 	T_{PSU}	XC4005L XC4010L XC4013L	21.0 20.0 19.0	18.0 17.0 16.0		ns ns ns
	(Min)					
Input Hold Time, using IFF (with delay) 	T_{PH}	XC4005L XC4010L XC4013L	0 0 0	0 0 0		ns ns ns
	(Min)					

OFF = Output Flip-Flop IFF = Input Flip-Flop or Latch

ADVANCED

XC4000L IOB Input Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000L devices unless otherwise noted.

	Speed Grade		-6		-5		-4	
Description	**Symbol**	**Device**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
Propagation Delays (CMOS Inputs)								
Pad to I1, I2	T_{PIDC}	All devices						
Pad to I1, I2 via transparent latch, no delay	T_{PLIC}	All devices						
with delay	T_{PDLIC}	XC4005L XC4010L XC4013L						
Propagation Delays (CMOS Inputs)								
Clock (IK) to I1, I2 (flip-flop)	T_{IKRI}	All devices		8.0		7.0		
Clock (IK) to I1, I2 (latch enable, active Low)	T_{IKLI}	All devices		8.0		7.0		
Hold Times (Note 1)								
Pad to Clock (IK), no delay	T_{IKPI}	All devices	1.0		1.0			
Pad to Clock (IK), with delay	T_{IKPID}	All devices	0		0			
Clock Enable (EC) to Clock (IK), no delay	T_{IKEC}	All devices						
with delay	T_{IKECD}	All devices						
Setup Times (CMOS Inputs)								
Pad to Clock (IK), no delay	T_{PICKC}	All devices						
with delay	T_{PICKDC}	XC4005L XC4010L XC4013L						
Setup Times (CMOS Inputs)								
Clock Enable (EC) to Clock (IK), no delay	T_{ECIK}	All devices						
with delay	T_{ECIKD}	XC4005L XC4010L XC4013L						
			ADVANCED					

Note 1: Input pad setup and hold times are specified with respect to the internal clock (IK). For setup and hold times with respect to the clock input pin, see the pin-to-pin parameters in the Guaranteed Input and Output Parameters table.

Note 2: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

XC4000L IOB Output Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000L devices unless otherwise noted.

Speed Grade		**-6**		**-5**		**-4**	
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
Propagation Delays (CMOS Output Levels)							
Clock (OK) to Pad, fast	T_{OKPOFC}						
slew-rate limited	T_{OKPOSC}						
Output (O) to Pad, fast	T_{OPFC}						
slew-rate limited	T_{OPSC}						
3-state to Pad hi-Z (slew-rate independent)	T_{TSHZC}						
3-state to Pad active and valid, fast	T_{TSONFC}						
slew-rate limited	T_{TSONSC}						
Setup and Hold							
Output (O) to clock (OK) setup time	T_{OOK}	8.0		6.0			
Output (O) to clock (OK) hold time	T_{OKO}	0		0			
Clock Enable (EC) to clock (OK) setup time	T_{ECOK}						
Clock Enable (EC) to clock (OK) hold time	T_{OKEC}						
Clock							
Clock High	T_{CH}	5.0		4.5			
Clock Low	T_{CL}	5.0		4.5			
Global Set/Reset (Note 3)							
Delay from GSR net through Q to I1, I2	T_{RRI}		14.5		13.5		
Delay from GSR net to Pad	T_{RPO}		18.0		17.0		
GSR width	T_{MRW}	21.0		18.0			
		ADVANCED					

Note 1: Timing is measured at pin threshold, with 50pF external capacitive loads (incl. test fixture). Slew-rate limited output rise/fall times are approximately two times longer than fast output rise/fall times. For the effect of capacitive loads on ground bounce, see the "Additional XC4000 Data" section of the Programmable Logic Data Book.

Note 2: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

Note 3: Timing is based on the XC4005L. For other devices see the XACT timing calculator.

XC4000L Boundary Scan (JTAG) Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements. For more detailed, more precise, and more up-to-date information, use the values provided by the XACT timing calculator and used in the simulator. These values can be printed in tabular format by running LCA2XNF -S.

The following guidelines reflect worst-case values over the recommended operating conditions. They are expressed in units of nanoseconds and apply to all XC4000L devices unless otherwise noted.

Speed Grade		**-6**		**-5**		**-4**	
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**
Setup and Hold							
Input (TDI) to clock (TCK) setup time	T_{TDITCK}						
Input (TDI) to clock (TCK) hold time	T_{TCKTDI}						
Input (TMS) to clock (TCK) setup time	T_{TMSTCK}						
Input (TMS) to clock (TCK) hold time	T_{TCKTMS}						
Propagation Delay							
Clock (TCK) to Pad (TDO)	T_{TCKPO}						
Clock							
Clock (TCK) High	T_{TCKH}						
Clock (TCK) Low	T_{TCKL}						
Power-On Reset							
JTAG operation after valid Vcc	T_{RJTAG}						
		ADVANCED					

Note 1: Input pad setup and hold times are specified with respect to the internal clock (IK). For setup and hold times with respect to the clock input pin, see the pin-to-pin parameters in the Guaranteed Input and Output Parameters table.

Note 2: Output timing is measured at pin threshold, with 50pF external capacitive loads (incl. test fixture). Slew-rate limited output rise/fall times are approximately two times longer than fast output rise/fall times. For the effect of capacitive loads on ground bounce, see the “Additional XC4000 Data” section of the Programmable Logic Data Book.

Note 3: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

XC4000EX Switching Characteristics

XC4000EX timing parameters were not available at the time this document was released. See the Xilinx WEBLINX at http://www.xilinx.com for the latest available information.

XC4000XL Switching Characteristics

XC4000EX timing parameters were not available at the time this document was released. See the Xilinx WEBLINX at http://www.xilinx.com for the latest available information.

Product Availability

Table 25 - Table 27 show the planned packages and speed grades for XC4000-Series devices. Call your local sales office for the latest availability information, or see the Xilinx WEBLINX at `http://www.xilinx.com` for the latest revision of the specifications.

Table 1: Component Availability Chart for XC4000E FPGAs

	Speed Grade	PC 84	PQ 100	VQ 100	PG 120	TQ 144	PG 156	PQ 160	CB 164	PG 191	CB 196	PQ 208	HQ 208	PG 223	BG 225	CB 228	PQ 240	HQ 240	PG 299	HQ 304
XC4003E	-4	C I	C I	C I	C I															
	-3	C	C	C	C															
	-2	C	C	C	C															
XC4005E	-4	C I	C I			C I	C I M B	C I	M B			C I								
	-3	C	C			C	C	C				C								
	-2	C	C			C	C	C				C								
XC4006E	-4	C I				C I	C I	C I				C I								
	-3	C				C	C	C				C								
	-2	C				C	C	C				C								
XC4008E	-4	C I						C I		C I		C I								
	-3	C						C		C		C								
	-2	C						C		C		C								
XC4010E	-4	C I						C I		C I MB	MB	C I			C I					
	-3	C						C		C		C			C					
	-2	C						C		C		C			C					
XC4013E	-4							C I				C I	C I	C I M B	C I	M B	C I	C I		
	-3							C				C	C	C	C		C	C		
	-2							C				C	C	C	C		C	C		
XC4020E	-4												C I	C I				C I		
	-3												C	C				C		
	-2												C	C				C		
XC4025E	-4													C I		M B		C I	C I M B	C I
	-3													C				C	C	C
	-2													C				C	C	C

C = Commercial, T_J = 0° to +85° C
I = Industrial, T_J = -40° to +100° C
M = Mil Temp, T_C = -55° to +125° C
B = MIL-STD-883C Class B, T_C = -55° to +125° C
Shaded device/package combinations are not supported.

Table 2: Component Availability Chart for XC4000EX FPGAs

	Speed Grade	HQ208	HQ240	PG299	HQ304	BG352	PG411	BG432
XC4028EX	-4	C I	C I	C I	C I	C I		
	-3	C	C	C	C	C		
	-2	C	C	C	C	C		
XC4036EX	-4				C I		C I	C I
	-3				C		C	C
	-2				C		C	C
XC4044EX	-4						C I	C I
	-3						C	C
	-2						C	C

C = Commercial, T_J = 0° to +85° C
I = Industrial, T_J = -40° to +100° C
M = Mil Temp, T_C = -55° to +125° C
B = MIL-STD-883C Class B, T_C = -55° to +125° C
Shaded device/package combinations are not supported.

Table 3: Component Availability Chart for XC4000L and XC4000XL FPGAs

	Speed Grade	PC84	TQ176	PQ208	BG225	PQ240	PQ304	BG352	BG432	PG499
XC4005L	-6	C		C						
	-5	C		C						
	-4									
XC4010L	-6	C	C	C						
	-5	C	C	C						
	-4									
XC4013L	-6			C	C	C				
	-5			C	C	C				
	-4									
XC4028XL										
XC4036XL										
XC4044XL										
XC4052XL										
XC4062XL										

C = Commercial, T_J = 0° to +85° C
I = Industrial, T_J = -40° to +100° C
M = Mil Temp, T_C = -55° to +125° C
B = MIL-STD-883C Class B, T_C = -55° to +125° C
Shaded device/package combinations are not supported.
Speed grades for the XC4000XL have not yet been determined.

Package Pinouts and Physical Dimensions

For XC4000E and XC4000L package pinouts and physical dimensions, see the ***Programmable Logic Data Book***. XC4000 pinouts apply to the corresponding XC4000E and XC4000L devices.

XC4028EX and XC4028XL package pinouts and physical dimensions are the same as the XC4025 and XC4025E. Package pinouts and physical dimensions for the larger XC4000EX/XL devices were not available at the time of this publication. See the Xilinx WEBLINX at `http://www.xilinx.com` for the latest revision of the specifications.

Maximum available user I/O for each device/package combination is shown in Table 28 - Table 30.

Table 4: Maximum User I/O for XC4000E Device/Package Combinations

No. of Pins	Package (Code)	XC4003E	XC4005E	XC4006E	XC4008E	XC4010E	XC4013E	XC4020E	XC4025E
Maximum User I/O		**80**	**112**	**128**	**144**	**160**	**192**	**224**	**256**
84	PLCC (PC)	61	61	61	61	61			
100	PQFP (PQ)	77	77						
	VQFP (VQ)	77							
120	PGA (PG)	80							
144	TQFP (TQ)		96	96					
156	PGA (PG)		112	125					
160	PQFP (PQ)		112	128	129	129	129		
164	CBFP (CB)		112						
191	PGA (PG)				144	160			
196	CBFP (CB)					160			
208	PQFP (PQ)		112	128	144	160	160		
	HQFP (HQ)						160	160	
223	PGA (PG)						192	192	192
225	BGA (BG)					160	192		
228	CBFP (CB)						192		192
240	PQFP (PQ)						192		
	HQFP (HQ)						192	193	193
299	PGA (PG)								256
304	HQFP (HQ)								256

Note: This table includes standard user-programmable I/O. It also includes the TDI, TCK, and TMS pins, which can function as user-programmable I/O if not used for boundary scan. In addition to the I/O listed in this table, the M0 and M2 pins can be used as inputs only; the M1 and TDO pins can be used as outputs only. All of these pins must be called out using special library symbols. The XACT software does not use them by default. (See Table 18 on page 42.)

Table 5: Maximum User I/O for XC4000EX Device/Package Combinations

No. of Pins	Package (Code)	XC4028EX	XC4036EX	XC4044EX
Maximum User I/O		**256**	**288**	**320**
208	HQFP (HQ)	160		
240	HQFP (HQ)	201		
299	PGA (PG)	256		
304	HQFP (HQ)	256	256	
352	BGA (BG)	256		
411	PGA (PG)		288	320
432	BGA (BG)		288	320

Note: This table includes standard user-programmable I/O. It also includes the TDI, TCK, and TMS pins, which can function as user-programmable I/O if not used for boundary scan. In addition to the I/O listed in this table, the M0 and M2 pins can be used as inputs only; the M1 and TDO pins can be used as outputs only. All of these pins must be called out using special library symbols. The XACT software does not use them by default. (See Table 18 on page 42.)

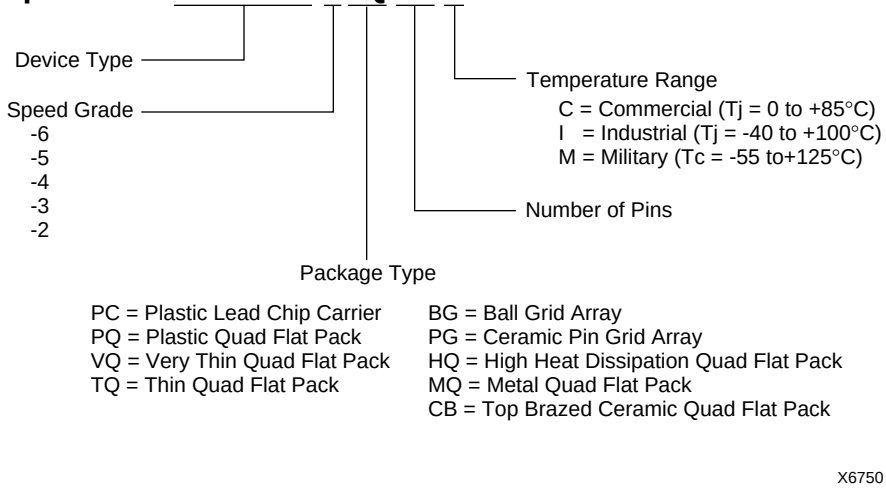
Table 6: Maximum User I/O for XC4000L and XC4000XL Device/Package Combinations

No. of Pins	Package (Code)	XC4005L	XC4010L	XC4013L	XC4028XL	XC4036XL	XC4044XL	XC4052XL	XC4062XL
Maximum User I/O		**112**	**160**	**192**	**256**	**288**	**320**	**352**	**384**
84	PLCC (PC)	61	61						
176	TQFP (TQ)		153						
208	PQFP (PQ)	112	160	160					
225	BGA (BG)			192					
240	PQFP (PQ)			192	201				
304	PQFP (PQ)				256	256			
352	BGA (BG)				256				
432	BGA (BG)					288	320	352	
499	PGA (PG)								TBD

Note: This table includes standard user-programmable I/O. It also includes the TDI, TCK, and TMS pins, which can function as user-programmable I/O if not used for boundary scan. In addition to the I/O listed in this table, the M0 and M2 pins can be used as inputs only; the M1 and TDO pins can be used as outputs only. All of these pins must be called out using special library symbols. The XACT software does not use them by default. (See Table 18 on page 42.)

Ordering Information

Example: **XC4013E-3HQ240C**



X6750

XILINX® The Programmable Logic Company℠

Headquarters

Xilinx, Inc.
2100 Logic Drive
San Jose, CA 95124
U.S.A.
Tel: 1 (800) 255-7778
or 1 (408) 559-7778
Fax: 1 (800) 559-7114

Net: hotline@xilinx.com
Web: http://www.xilinx.com

North America

Irvine, California
(714) 727-0780

Sunnyvale, California
(408) 245-9850

Schaumburg, Illinois
(847) 605-1972

Nashua, New Hampshire
(603) 891-1096

Raleigh, North Carolina
(919) 846-3922

West Chester, Pennsylvania
(610) 430-3300

Dallas, Texas
(214) 960-1043

Europe

Xilinx Sarl
Jouy en Josas, France
Tel: (33) 1-34-63-01-01
Net: frhelp@xilinx.com

Xilinx GmbH
Aschheim, Germany
Tel: (49) 89-99-1549-01
Net: dlhelp@xilinx.com

Xilinx, Ltd.
Byfleet, United Kingdom
Tel: (44) 1932-349401
Net: ukhelp@xilinx.com

Japan

Xilinx, K.K.
Tokyo, Japan
Tel: (03) 3297-9191

Asia Pacific

Xilinx Asia Pacific
Hong Kong
Tel: (852) 2424-5200
Net: hongkong@xilinx.com