

Complete ISP™
Development Kits
Starting at Only \$99

ispStarter Kits

Complete Sets of Software, Hardware,
Datasheets and Samples for Lattice ISP™ Devices

ispStarter™ Kits Include

Software

- Choice of Two Logic Development Systems: pDS® Starter or pDS+™ ABEL Starter Software for ispLSI® 1016 and ispLSI 2032 Devices
- ispGDS™ (Generic Digital Switch) Compiler Software
- ispCODE™ — C++ Source In-System Programming Routines
- isp Daisy Chain Download Software

Samples

- ispLSI 2032-80LJ Device in 44-pin PLCC
- ispGAL®22V10B-15LJ Device in 28-pin PLCC
- ispGDS14-7J Device in 20-pin PLCC

Hardware

- ispDOWNLOAD™ Cable

1994 Lattice Data Book

In-System Programmability™ Manual

ispLSI and pLSI 2032 Datasheet

Features

- Easy-to-Use Kit Contains Everything Needed for In-System Programmable Device Design-in
- Supports Lattice's ispLSI 1016 and ispLSI 2032 Devices — the Industry's Fastest High Density Programmable Devices at up to 7.5ns t_{PD} and 135 MHz F_{max}
- Supports Industry Standard 22V10 Architecture Coupled with Lattice's Innovative In-System Programmable Capability
- Supports Lattice's New ISP Generic Digital Switch for Applications such as Software Driven Hardware Configuration and Multiple DIP Switch Replacement

The ispStarter Kits are designed to make Lattice's innovative in-system programmable device technology available in a single, complete package. The ispStarter Kits contain all the software, hardware, device samples, and information you need to begin designing with Lattice's ISP products. The ispLSI devices are the fastest High Density Programmable Logic devices in the industry at up to 7.5ns and 135MHz. Lattice's new 7.5ns ispGAL22V10 device has all the advantages of In-System Programmability and maintains the familiar 22V10 architecture and 28-pin PLCC pinout. The ispGDS™ is Lattice's latest in-system programmable innovation. This new family of devices offers the ability to configure its programmable switch matrix to connect signals arbitrarily between two banks of I/O pins or to force pins to fixed high or low logic states.

In-System Programmability (ISP)

ISP is a Lattice innovation that supports device function programming and reprogramming on the printed circuit board at 5 volts. There are several advantages to in-system programmability: First, it accelerates the system and board level debug process and enables you to define your board layout earlier in the design process. Second, ISP eliminates bent leads caused by extra handling and socket insertions made during the device programming process. Third, systems incorporating ISP are reconfigurable with the devices already soldered to the p.c. board, minimizing board rework time and expense. With this capability your system options are boundless and easier field updates are made possible by downloading a new configuration file via a floppy disk or modem.

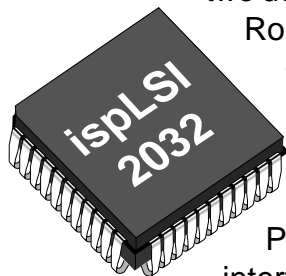


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ispLSI 2032 and Lattice Design Software (Supports ispLSI 2032 and ispLSI 1016)

Available in speed grades from 7.5ns to 15ns t_{PD} and 80MHz to 135MHz F_{max} , the ispLSI 2032 device is a fast, high density programmable logic device containing 32 logic macrocells, 32 Universal I/O pins, two dedicated input pins, three dedicated clock input pins, and a programmable Global Routing Pool (GRP). The basic logic element of the device is the Generic Logic Block (GLB) which has 18 inputs, a programmable AND/OR/XOR array, and four outputs that may be configured as either combinatorial or registered.

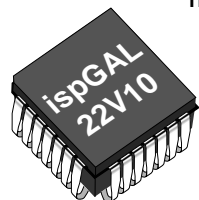


Lattice's pDS Starter Software for ispLSI 2032 and ispLSI 1016 devices is a high performance development environment that runs on IBM compatible 386/486/Pentium™ PCs. The software has a friendly, efficient, Microsoft Windows™ user interface which supports familiar Boolean equation entry. pDS features automatic Place and Route for quick design implementation. To make designing even easier there is a library of over 200 Logic Macros for fast design entry.

For ABEL users, Lattice's pDS+ ABEL Starter Software for ispLSI 2032 and ispLSI 1016 devices works with ABEL 4.3 or later and performs efficient design optimization and minimization, plus automatic partitioning and place and route for high device utilization.

ispGAL22V10

The ispGAL22V10 is the industry's first in-system programmable 22V10 device and offers speeds from 7.5ns to 15ns maximum propagation delay. The generic architecture provides maximum flexibility by allowing the Output Logic Macrocell (OLMC) to be configured by the user.

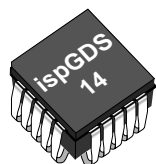


The logic functionality, fusemap, and AC and DC parameters of the ispGAL22V10 are fully compatible with standard bipolar and CMOS 22V10 devices. The 28-pin PLCC package provides the same functional pinout as the standard 22V10 by using the four "No Connect" pins on the 28-pin PLCC for the ISP interface signals.

Designs for the ispGAL22V10 can be compiled by any logic compiler supporting the 22V10 architecture. The isp Daisy Chain Download Software takes any 22V10 JEDEC file as input and programs the device, in-system, quickly and easily.

ispGDS and Compiler

The Lattice ispGDS family is an ideal solution for reconfiguring system signal routing and replacing DIP switches used for feature selection. Each I/O cell can be configured as an input, an inverting or noninverting output, or a fixed TTL high or low output. Any I/O pin in one bank can be driven by any I/O pin in the opposite bank with only a 7.5ns total signal delay. A single input can also drive one or more outputs in the opposite bank, allowing a signal, such as a clock, to be distributed to multiple destinations on the board.



The ispGDS Compiler is a simple text entry and compilation tool. isp Daisy Chain Download Software gives you the ability to program ispGDS devices while they remain soldered to the p.c. board.

Ordering Information

| Part Number | Description | Price |
|--------------------|---|--------------|
| isp-SK2 | Lattice ispStarter Kit (Stand-alone MS Windows based) | \$99.00 |
| isp-SK2/ABEL | Lattice ispStarter Kit/ABEL (For use with ABEL 4.3 or higher) | \$199.00 |